TI Report No.
03-65-81

TEXAS INSTRUMENTS INCORPORATED
Semiconductor-Components Division
P.O. Box 5012
Dallas, Texas, 75222

TECHNICAL SUMMARY REPORT
ON
THE STUDY OF THE EPITAXIAL PARAMETERS ON RELIABILITY OF SILICON PLANAR DEVICES

(25 June 1964 to 25 June 1965)

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This report was prepared by Texas Instruments Incorporated under Contract No. NAS8-11330 for the George C. Marshall Space Flight Center of the National Aeronautics and Space Administration. The work was administered under the technical direction of the Astrionics Laboratory of the George C. Marshall Space Flight Center with Mr. Alvis M. Holladay acting as project manager.

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ABSTRACT

The effect of epitaxial parameters on the reliability of silicon planar devices has been investigated. The properties of the silicon substrates, substrate surface preparation, and growth conditions for the epitaxial layers were varied. High reliability, npn, double-diffused, epitaxial planar silicon transistors (2N2432) were fabricated from layers deposited under different conditions. Power step-stress tests, temperature only step-stress tests, high temperature storage tests and various materials investigations were carried out. No correlation between the material and process parameters involved in the growth of epitaxial layers on silicon substrates and the ultimate reliability of the low-voltage, small-signal devices fabricated from these layers was observed. From this, it can be concluded that present epitaxial deposition processes are quite satisfactory for this type of device. It cannot be concluded, however, that the reliability of large area, high voltage, high power devices is not affected by deposition conditions. Suggestions are made relating to the future directions of similar programs.

FOREWORD

The work reported herein was carried out primarily in the Semiconductor Research and Development Laboratory of the Semiconductor Components Division of Texas Instruments Incorporated. The project engineer was M. Bullis. Substantial contributions to the program were made by the following individuals: J. Sherer and R. Yeakley, substrate polishing and cleaning; C. Allen, epitaxial deposition and thermal resistance measurements; S. Watelski, surface examination and etch pits counts; W. Phillips, second breakdown measurements; W. Runyan, model analysis; D. Little, diffusion of slices for electrical measurements; D. Briggs, power step-stress tests. The devices were fabricated in the Silicon Small Signal Department under the supervision of B. Snow, E. Domel, and A. Canterbury. J. Martin, of the Silicon Small Signal Department, coordinated the storage step-stress tests. K. Howard, of the Central Analytical Facility, performed the x-ray topographic studies. Contract administrators were R. Haire and R. Kinsey. The second breakdown measurements were made on equipment designed and built by W. Portnoy. Portions of this report were prepared by W. Runyan, by W. Phillips, and by M. Bullis.

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I. TECHNICAL DISCUSSION

A. PURPOSE OF STUDY

Epitaxially deposited silicon layers are being used more and more for the fabrication of discrete devices and integrated circuit structures. Control of collector resistance in a discrete device and improved isolation between components of an integrated circuit are some of the advantages which can be obtained by using epitaxially deposited layers. As techniques become more sophisticated, additional advantages such as selective deposition in defined areas to obtain desired electrical characteristics are being realized. The increased use of these layers requires the development of additional fundamental knowledge about their properties.

This research study was undertaken to obtain a more complete understanding of the relationship between the reliability of simple solid state devices made from epitaxial silicon and the materials and process parameters involved in the growth of epitaxial layers on silicon substrates. In particular, the characteristics of the silicon crystal substrate, the surface preparation of the substrate, and growth conditions for the epitaxial layer were to be considered.

By observing the reliability of devices made from epitaxial layers deposited under various conditions, it was intended to determine the conditions for optimum epitaxial growth in terms of presently known technology. Correlations between device reliability and other material and device characteristics were to be made wherever possible in order to identify the origins of failure. With the results of these tests, it was expected that a selection of the conditions which will most likely provide maximum reliability of the finished device could be made.

B. LITERATURE SURVEY

At the beginning of the contract period, the literature was surveyed for pertinent references in the subject area. Although much work has been done and many papers have been written concerning semiconductor device reliability, the literature on the effects of bulk characteristics is very sparse. No reports dealing specifically with the effects of epitaxial parameters on device reliability were found.

Much of the applicable literature has resulted from the Physics of Failure Program sponsored by Rome Air Development Center. Several papers were presented at the 1963 Physics of Failure in Electronics Conference in Chicago. Solid-state diffusion of indium in germanium at about 100°C was shown to reduce the base width in a surface barrier transistor by 0.8μ in 1000 hours.[1] Mann and Sandler[2] suggested that dislocations generated by the addition of large concentrations of impurities in silicon may enhance the probability of failure when the structure is subjected to a mechanical or thermal stress. They postulated that the weakest plane occurs at approximately 1/3 the total diffusion depth and that the effect can be reduced by reducing the surface concentration and subsequently reducing the maximum concentration gradients in the diffused structure.

Thomas and Gorton[3] suggested that copper may be the predominant impurity which controls the carrier lifetime and reverse current in silicon between 85 and 200°C. It is possible that copper precipitation may occur which results in hot spots

and breakdown. Similar hot spots have been studied extensively under RADC contract AF 39(602)-3016 at Shockley Transistor Laboratory.[4] Queisser[5] showed that there is an enhancement of metallic precipitation at stair-rod dislocations associated with stacking faults in silicon, and that microplasmas occur at these dislocations.

At the 1964 Physics of Failure Conference, Gorton and Duchamp[6] suggested that measurable changes in net impurity concentration occur in the vicinity of the junction but no evidence of degradation of device characteristics was noted. Workman[7] observed gold flow from contacts into junction regions of devices after excessive stress. This is caused by local heating above the gold-silicon eutectic point at the contact and often results in emitter-base or emitter-collector shorts.* Bergh[8] found that contamination during power aging of double-diffused silicon npn mesa transistors in the presence of hydrogen and metallic copper resulted in deterioration of emitter junction characteristics and current gain which could be improved only by etching the bulk silicon.

During the course of the contract, it became clear that three relatively new techniques would yield more information concerning the effect of bulk parameters on device reliability than would conventional device studies. The first of these is

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* This failure mode was observed in the present study and will be discussed in more detail subsequently.

x-ray topography, a non-destructive technique for examining defects in silicon slices. This has been recently discussed in detail by Schwuttke.[9] The technique of reflection x-ray topography has been recently modified by Howard and Dobrott[10] specifically for the purpose of studying large area epitaxial films independently of the substrate.

The second breakdown effect in transistors has been discussed in detail by Schafft and French.[11] A non-destructive method of measurement introduced by Portnoy and Gamble[12] makes the study of this effect in many devices practical. It appears that detailed study of this effect will yield useful information in the present context.

Finally, a method proposed by H. Benda[13] for finding the intrinsic carrier concentration from transistor characteristics may prove useful in separating bulk and surface effects.

C. PRELIMINARY CONSIDERATIONS

Any relationships between materials and process parameters involved in the growth of epitaxial layers on silicon substrates and the ultimate reliability of devices fabricated from the layers will manifest themselves through changing device characteristics which result from the presence of something (e.g., chemical impurities, dislocations, stacking faults, etc.) introduced before or during the deposition. We will consider first some specific effects and impurities which might possibly be expected to cause such changes in device characteristics. When examining these, it is arbitrarily assumed that they must be able to contribute to degradation in the temperature range of from -55 to +300°C.

1. Effects

a. Diffusion: Fast diffusion of some chemical elements could lead to a undesired impurity distribution. This might be caused either by an unwanted impurity with a high diffusion coefficient or by diffusion enhancement from electric fields or structural imperfections. Preliminary work has indicated only a 10 per cent increase in the diffusion coefficient of boron when the dislocation density changed by 5 orders of magnitude,[14] but locally it must be much more severe. No increase in diffusion rate has been reported along stacking faults, but an appreciable increase has been observed along low angle grain boundaries.[15]

b. Precipitation: Many impurities precipitate along crystal imperfections. This can lead to changes in the electrical behavior of the silicon since the effect of impurities usually depends on the manner in which they are distributed.

c. Changing Mechanical Stress: If the stress becomes great enough, structural failure occurs, but even for stresses considerably less, the electrical properties can be appreciably affected. In particular, the reverse current and the forward voltage drop of diodes can be increased considerably.[16] There is, however, little data available on the relation between structure and either breaking stress or the magnitude of p-n junction degradation.

2. Specific Impurities

a. Oxygen: Oxygen can be introduced into silicon either during the crystal growing operation or by diffusion. Once in the lattice it can occupy either electrically active or inactive sites, depending on the annealing cycle. The net carrier concentration can thus be changed by the choice of cycles.

If the crystal is grown from a silica container (the normal Czochralski process) it will be saturated with oxygen and contain about 10^{18} atoms/cm^3. Presumably, similar amounts could be introduced by diffusion but this has not been extensively studied. The diffusion coefficient has been

determined, however, and is approximately 1 x 10^{-9} cm^2/sec at 1300°C.[17] In the as-grown crystal, oxygen is electrically inactive. However, by heating in the range from 300 to 450°C, the oxygen begins to form chains with the silicon, becomes active, and supplies an appreciable number of electrons. Continued heating causes the number of oxygen atoms per group to pass some critical number after which the aggregate again becomes electrically inactive. If instead of an extended heating at low temperatures, the silicon is heated to approximately 1000°C, the oxygen is all converted to the large-aggregate inactive species and no further heating at lower temperatures will change its behavior. However, by raising the temperature to near the melting point, the aggregates of oxygen will redissolve and the behavior is returned to the as-grown condition. Thus if devices are made from silicon containing oxygen, and have not been stabilized by heating above 1000°C, it is possible for continued storage at 300°C to change the bulk resistivity appreciably. This is shown in Fig. C-1.[18]

Because oxygen is a rather fast diffuser, it is possible for it to diffuse from an oxygen-containing substrate into an epitaxial layer during deposition, or from a surface oxide into an oxygen-free slice during the manufacture of planar devices. Figure C-2 shows the calculated oxygen distribution after a three-hour diffusion at 1150°C (D = 2 x 10^{-10} cm^2/sec) from a 10^{18} atoms/cm^3 substrate source. In this calculation, an infinitely thick layer was assumed. It indicates that at 20 microns from the substrate the oxygen concentration is approximately 10^{17} atoms/cm^3. In the

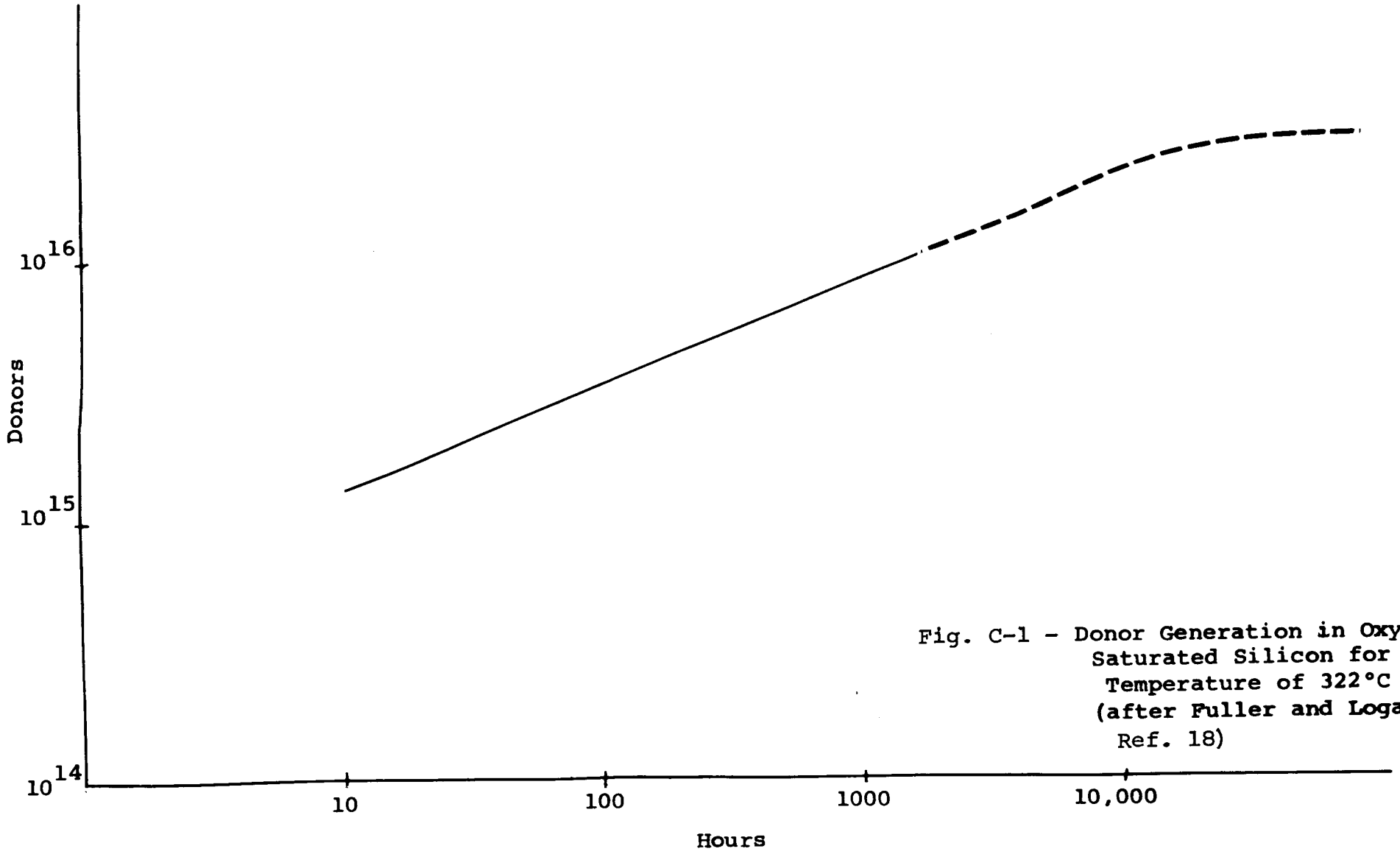
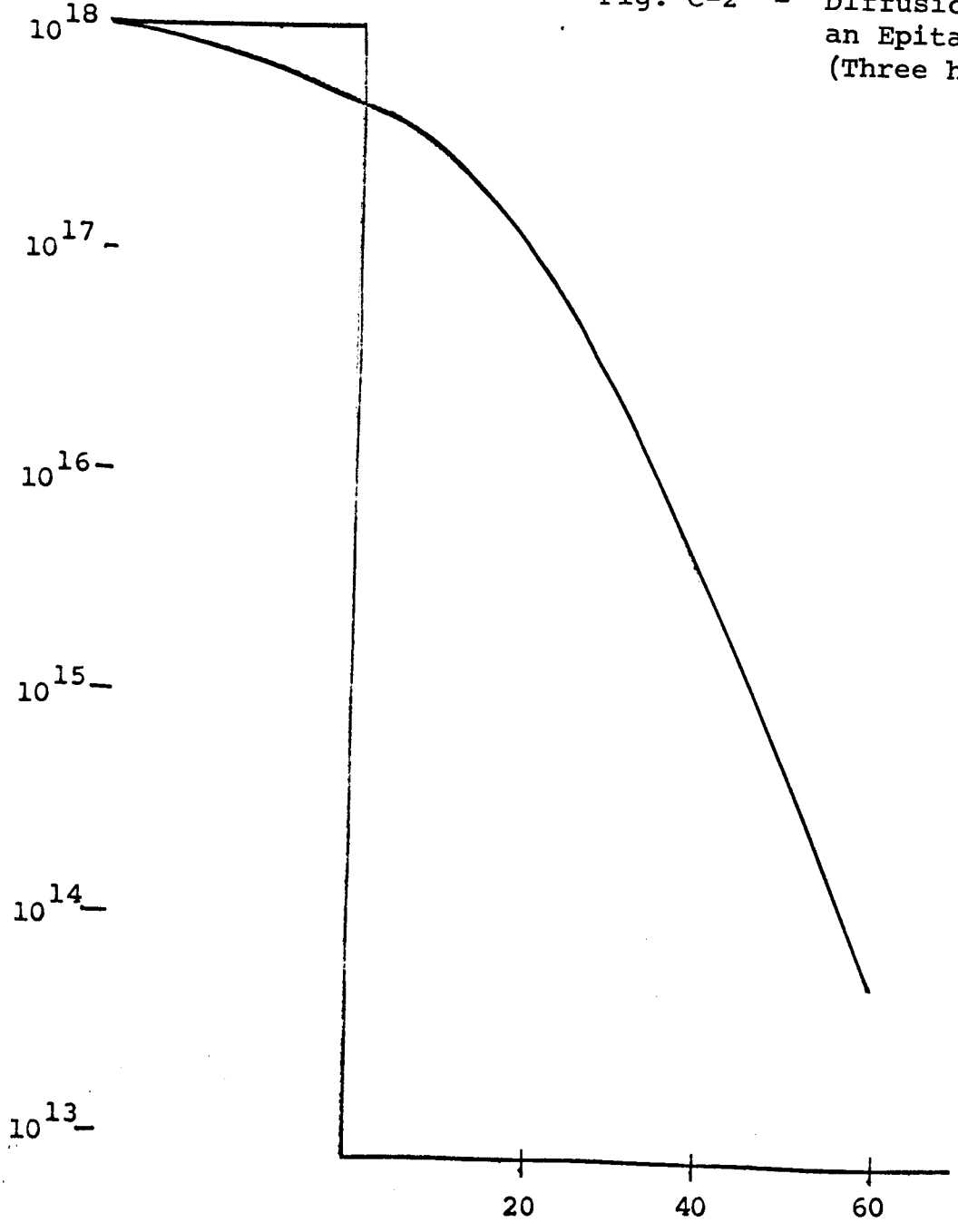


Fig. C-1 - Donor Generation in Oxygen Saturated Silicon for a Temperature of 322°C (after Fuller and Logan Ref. 18)

Fig. C-2 - Diffusion of Oxygen Into an Epitaxial Layer (Three hours at 1150°C)



event the layer is of finite thickness, and indeed most layers are less than 20 microns thick, the concentration at any given distance is greater than for the infinite case. It can thus be concluded that unless epitaxial layers are grown on oxygen-free substrates, the layer will have a high concentration of oxygen diffused into it by the time the diffusion steps associated with device fabrication are completed.

Calculations for the case of diffusion from an oxide layer could not be made because of lack of information pertaining to the transfer of oxygen atoms across the oxide-silicon boundary.

Fortunately, during manufacturing, most devices are subjected to enough high temperature processing (e.g., during diffusion) to stabilize them and render the oxygen inactive. However, some rather special devices, e.g., solar cells (having a very short, low temperature diffusion cycle), and grown junction transistors, may be susceptible to this effect.

b. Chlorine: Although epitaxial layers grown on oxygen-free substrates are free of oxygen, they do contain appreciable quantities of chlorine (over 10^{16} atoms/cm^3)*. There is little data available on the electrical behavior of chlorine in silicon, but as an exploratory project, a 10 mil thick epitaxial layer with an original resistivity of 130 ohm-cm, p-type, has been subjected to the heating cycle shown in Fig. C-3 with no observable change in resistivity.

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* The value was determined by neutron activation analysis (J. Nunn and J. Weaver, unpublished data).

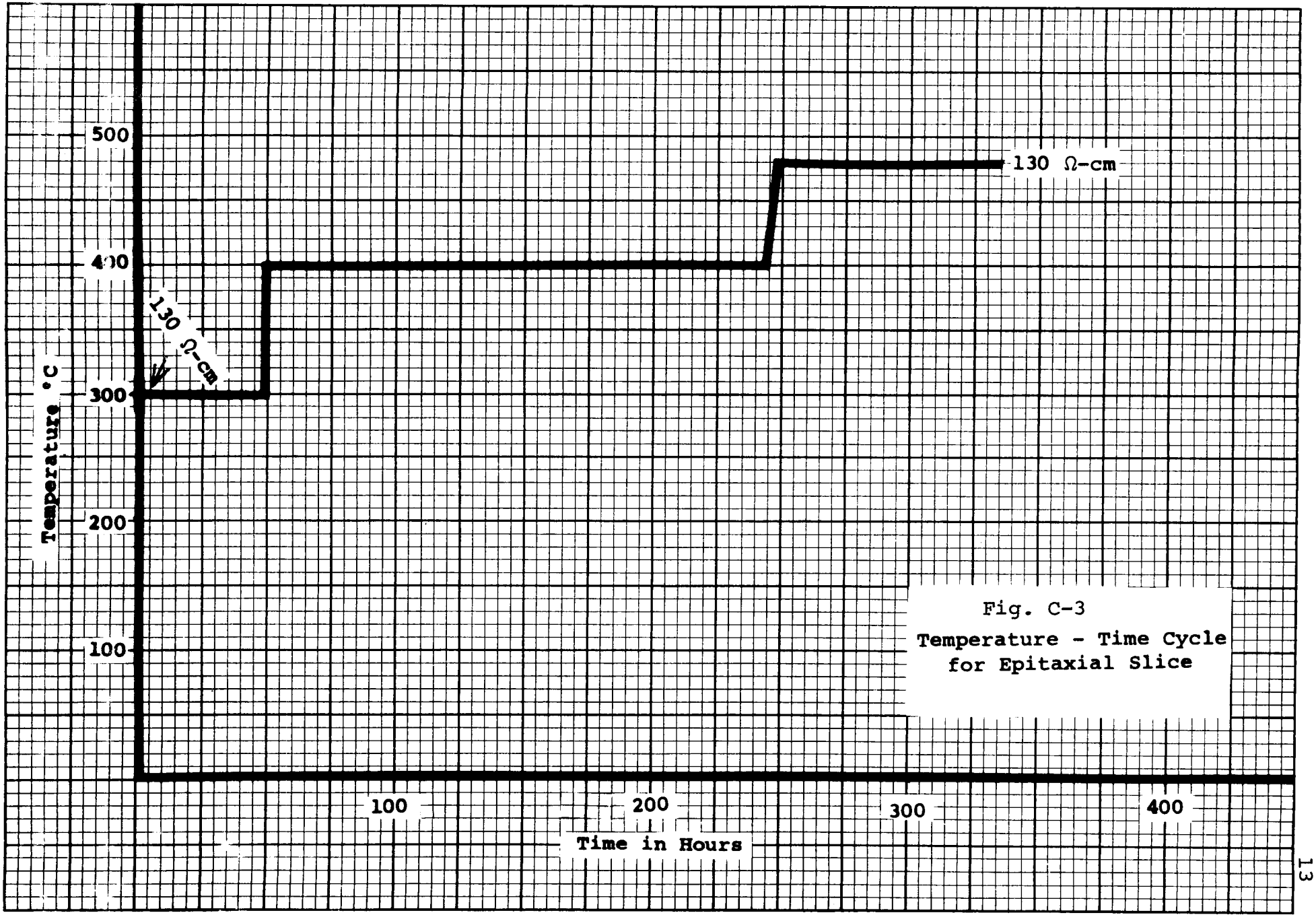

Fig. C-3
Temperature - Time Cycle
for Epitaxial Slice

c. Lithium and Sodium: Lithium is a known fast diffuser, but there seems to be little likelihood of its being accidentally introduced into the device. Sodium is likely to be present around silicon devices and is known to affect adversely their characteristics by drifting in oxide layers. However, its solubility and electrical activity in bulk silicon appears to be lower than would be observed in ordinary devices.

d. Gold: Gold is a fast diffuser, its diffusion coefficient is structure dependent, it is almost always present in small quantities, and it affects both resistivity and minority carrier lifetime. There are three ways in which movement of gold while the device is in operation might affect operation: (1) small amounts on the surface, from contacts for example, might diffuse into the base region and reduce lifetime; (2) gold deliberately introduced to kill lifetime might precipitate, become electrically inactive, and thus increase switching time; or (3) precipitation could introduce recombination centers into the space charge region and lead to an increase in the reverse current.

Gold diffusions in silicon are more involved than those of the usual III-A or V-A elements because gold may occupy either substitutional or interstitial sites, and with each of these locations there is a different diffusion coefficient:[19]

$$D_{substitutional} = 2.75 \times 10^{-3} \exp(-47{,}000/RT) \text{ cm}^2 \text{ sec}^{-1}$$

$$D_{interstitial} = 2.44 \times 10^{-4} \exp(-8{,}900/RT) \text{ cm}^2 \text{ sec}^{-1}$$

$$\left.\begin{matrix}\text{Substitutional} \\ \text{Solubility}\end{matrix}\right\} = 8.15 \times 10^{22} \exp(-40{,}600/RT) \text{ cm}^{-3}$$

$$\left.\begin{matrix}\text{Interstitial} \\ \text{solubility}\end{matrix}\right\} = 5.95 \times 10^{24} \exp(-58{,}000/RT) \text{ cm}^{-3}$$

Because the substitutional solubility exceeds the interstitial solubility by a large amount (as shown in Fig. C-4) while the diffusion coefficient for interstitial gold is much greater than that for substitutional gold, it is necessary to consider the dissociation reaction:

$$Au_{interstitial} + Vacancy \rightleftarrows Au_{substitutional}$$

and the vacancy generation rate. Under certain conditions, the diffusion of gold can be described by coefficients intermediate between those given above (as shown in Fig. C-5). Examination of the diffusion coefficients shows that appreciable diffusion might be expected to take place at temperatures as low as 300°C. However, the combined substitutional-interstitial solubility appears to be so low that the total amounts of gold involved at temperatures below 300°C would not be harmful to devices. This is based on two separate sets of high temperature data which extrapolate to 10^7 to 10^8 atoms/cm^3 at 300°C.

If it is assumed that the lifetime of gold doped silicon is given by $\frac{1}{\tau_f} = \frac{1}{\tau_o} + \frac{1}{\tau_{Au}}$, where τ_f is the final lifetime, τ_o is the original lifetime, and τ_{Au} is given by $\tau_{Au} = \frac{2.53 \times 10^7}{N_{Au}}$ for small gold concentrations, 10^{20} 10^8 atoms of gold/cm^3 would have negligible effect on even the longest lifetime material now in use. Examination of the calculated curves of resistivity vs gold concentration for various N_D and N_A show that 10^8 gold atoms/cm^3 would not affect resistivity. (See Figs. C-6 and C-7) From these considerations it is concluded that there is no likelihood, even with enhanced diffusion, of affecting material or device parameters by the diffusion of gold into regions where it is not desired.

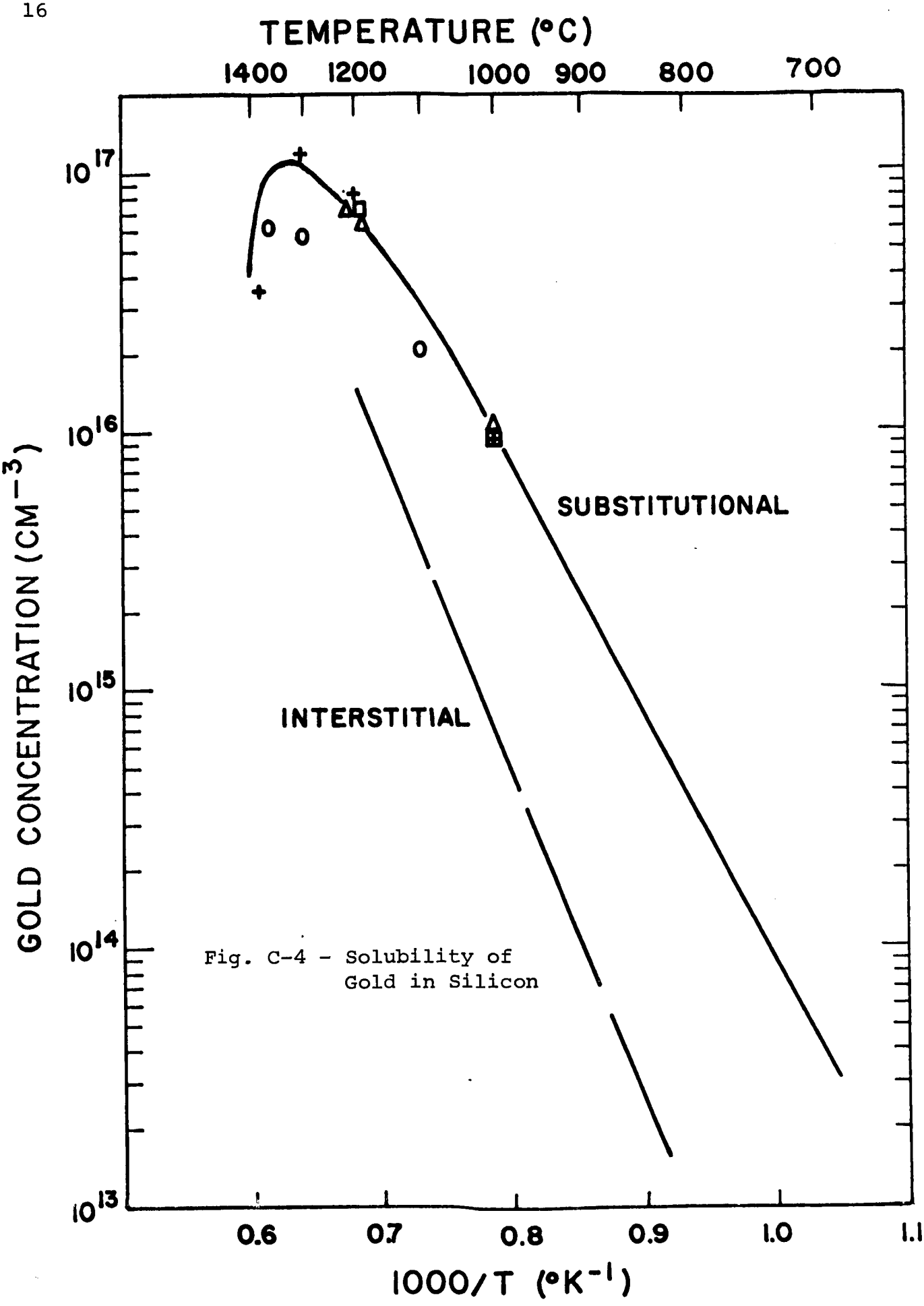

Fig. C-4 - Solubility of Gold in Silicon

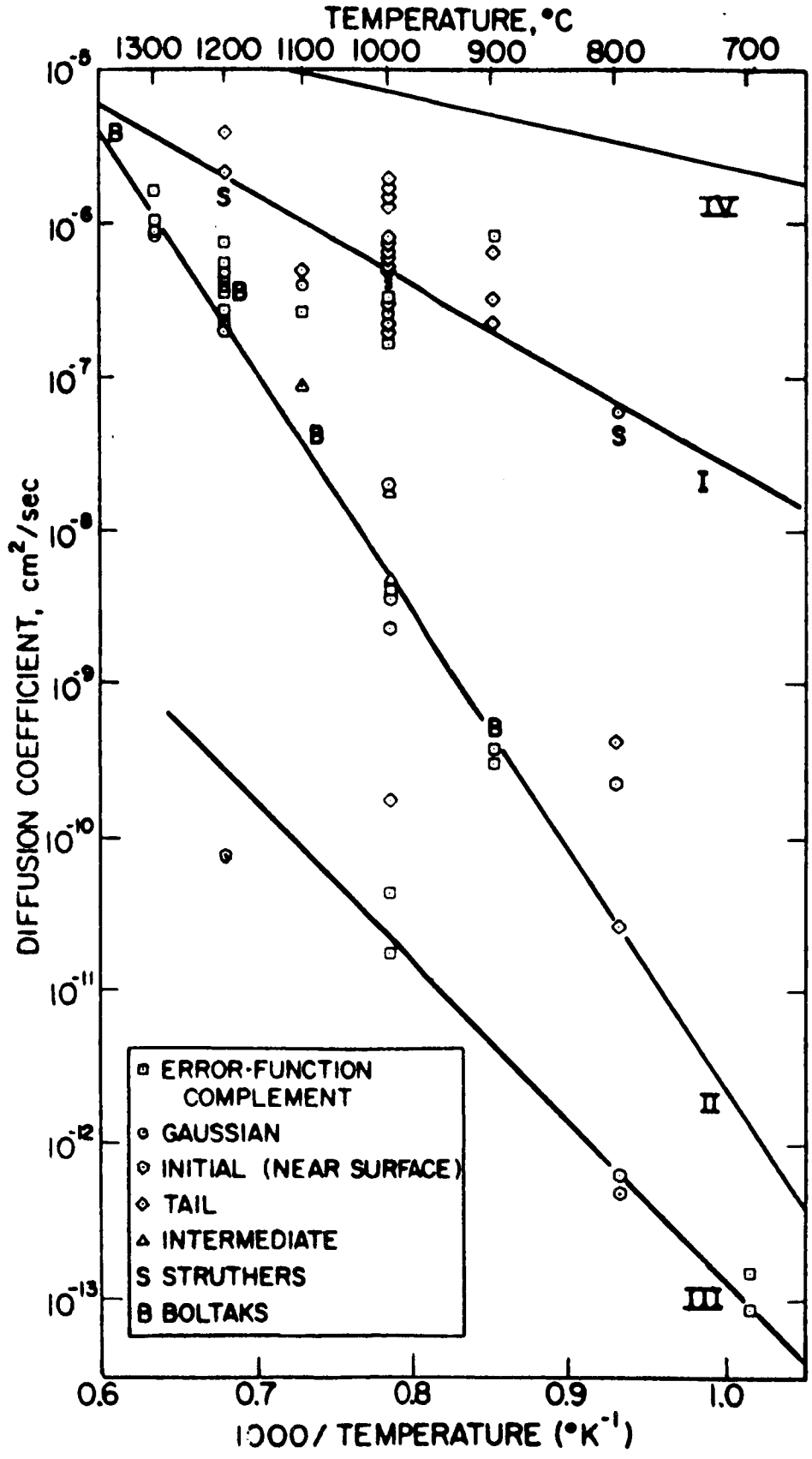

Fig. C-5 - Diffusion Coefficients of Gold in Silicon I. Interstitial Controlled Dissociative Diffusion; II. Vacancy Controlled Dissociative Diffusion; III. Substitutional Diffusion; IV. Interstitial Diffusion (after Wilcox and LaChapelle, Ref. 19).

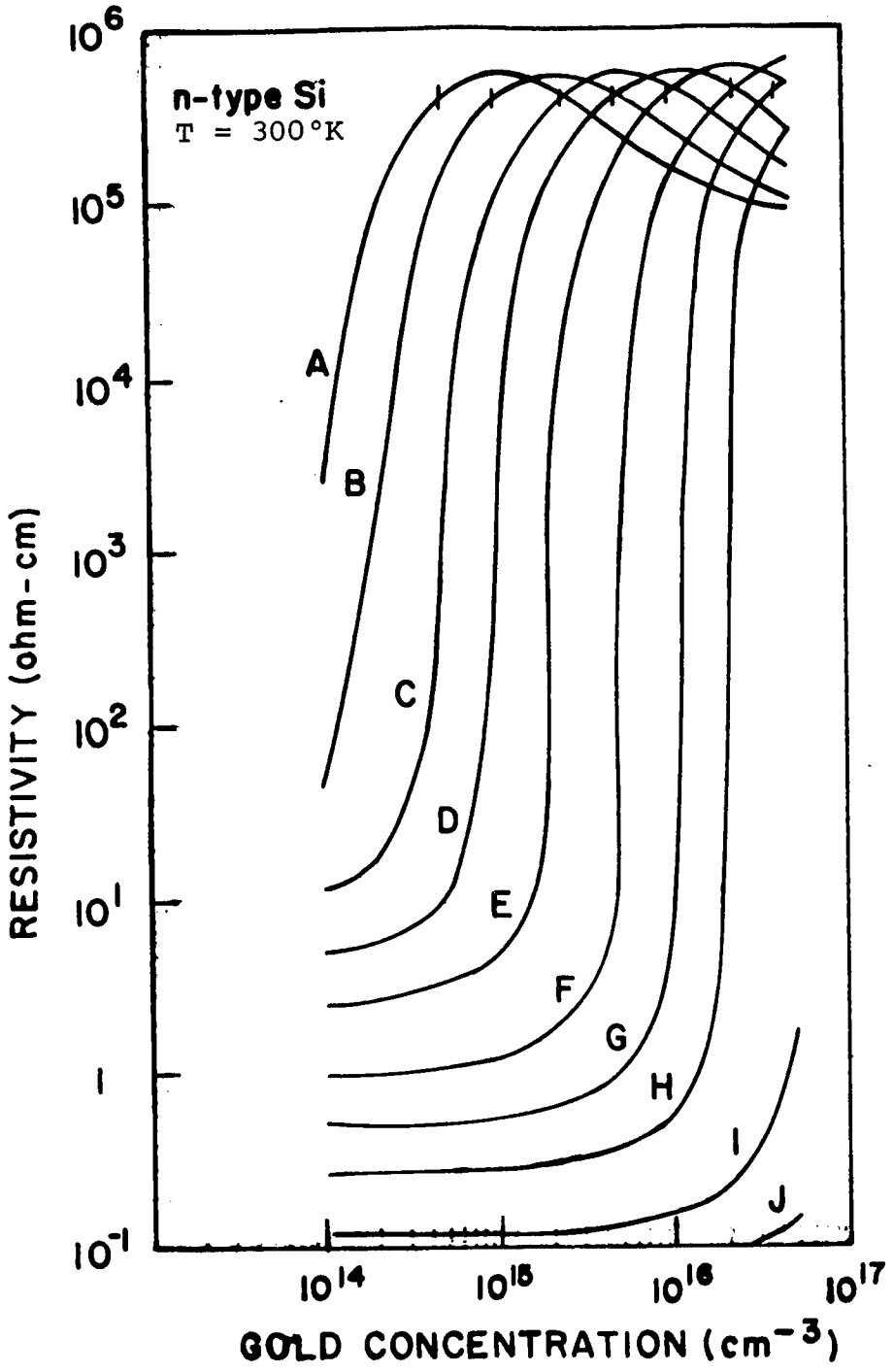

Fig. C-6 - Resistivity of n-type Silicon Doped with Gold. Shallow Donor Concentrations (cm^{-3}): A, 1×10^{14}; B, 2×10^{14}; C, 5×10^{14}; D, 1×10^{15}; E, 2×10^{15}; F, 5×10^{15}; G, 1×10^{16}; H, 2×10^{16}; I, 5×10^{16}; J, 1×10^{17}. To the right of the vertical bar on each curve $p > n$.

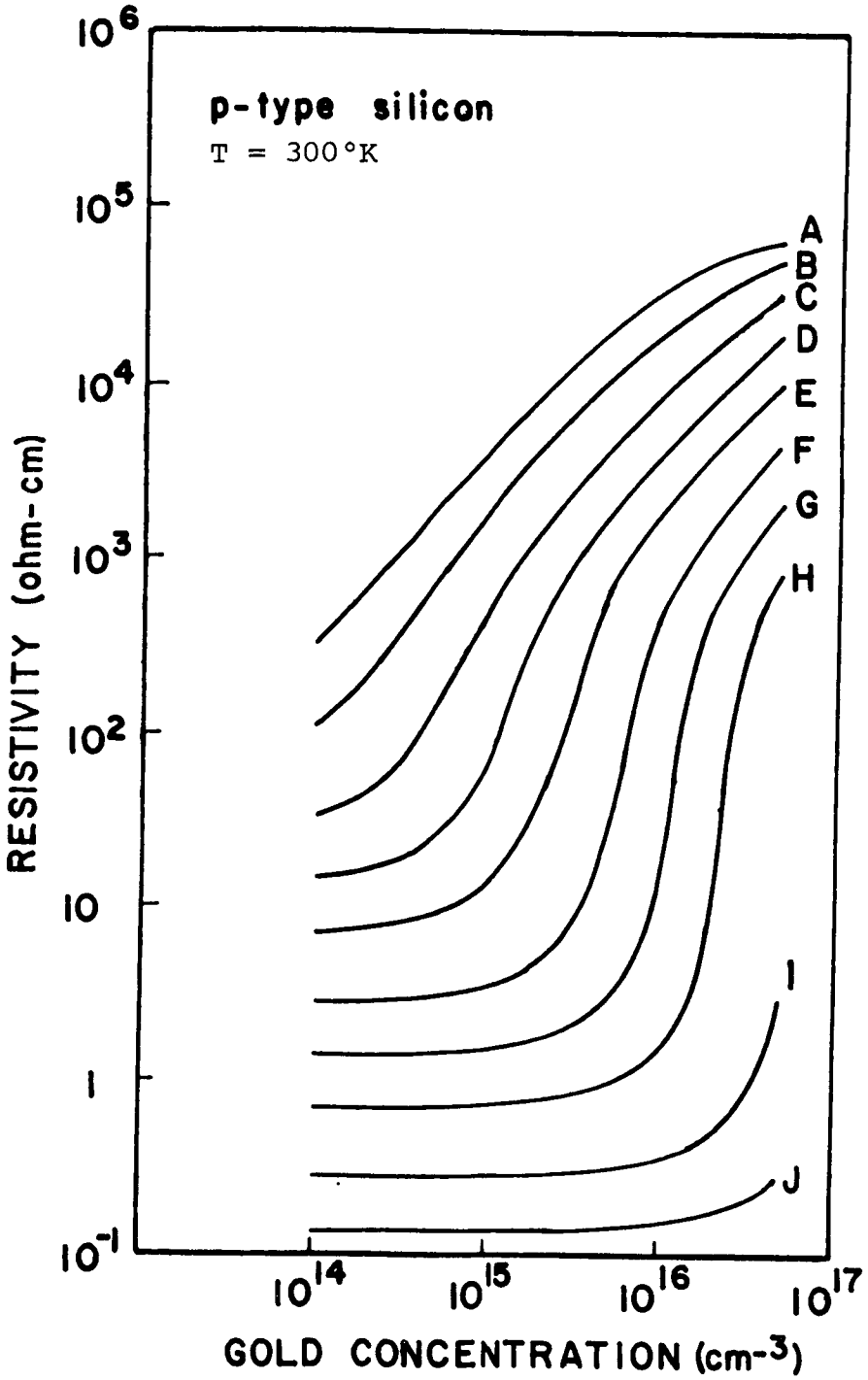

Fig. C-7 - Resistivity of p-type Silicon Doped with Gold. Shallow Acceptor Concentrations (cm^{-3}): A, 1×10^{14}; B, 2×10^{14}; C, 5×10^{14}; D, 1×10^{15}; E, 2×10^{15}; F, 5×10^{15}; G, 1×10^{16}; H, 2×10^{16}; I, 5×10^{16}; J, 1×10^{17}.

Specific attempts were made to observe gold precipitation in silicon. Gold was diffused into bulk slices and epitaxial layers at times and temperatures expected to result in a gold concentration of about 10^{16} cm^{-3}. Initial impurity densities were less than 5×10^{18} cm^{-3} in all cases. The slices were cooled rapidly from the diffusion temperature and then examined under an infrared optical transmission microscope using a standard Unitron microscope to which a Varo Miniscope* was added. Difficulties in diffusing the gold were encountered, and it is not certain the expected amount actually entered the slices. However, results in the literature also indicate that no precipitation would be expected at these impurity levels.

Dash[21] has studied the interaction of gold and dislocations in silicon. During the course of this study he investigated the effect of cooling rates and found no observable precipitation of gold after slow cooling the wafers from diffusion temperature. Radiotracer studies using Au^{198} diffused into silicon with a non-uniform dislocation density showed no evidence of precipitation of gold on dislocations even though the density of gold was greater in the area of greater dislocation density.

Wilcox, LaChapelle, and Forbes[22] found no precipitation with a variety of cooling cycles. They did notice a variation in the amount of out-diffusion from relatively thin surface layers. A variety of experiments,[20,23,24] in which counted and electrically active concentrations were observed to be equal also would appear to indicate that significant amounts of gold do not precipitate.

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* Infrared-visible image converter.

e. Others: Copper is known to precipitate in silicon and is likely to be a cause of difficulties. Silver would be expected to behave similarly to gold. The transition elements such as iron are less well understood, but are often fast diffusers, and also may produce unwanted precipitates.

D. PARAMETERS VARIED IN THE EPITAXIAL DEPOSITION

The main part of the study consisted of experiments designed to bring out any correlations between deposition conditions and device reliability which might be present. An extensive matrix of variables was designed and epitaxial layers were deposited on substrates under a wide variety of conditions. These layers were then used to fabricate test devices and/or for materials studies.

Variations in the various parameters were made as shown in Table D-I. All layers were n-type, approximately 5 ohm-cm, and were deposited by the hydrogen reduction of silicon tetrachloride ($SiCl_4$). In most cases the deposits were made on n-type substrates. In some instances, p-type substrates were also employed in order to obtain layers on which electrical measurements could be made directly.

A deposition cycle consisted of loading the substrate(s) into the reactor, purging the reactor with helium or forming gas, heating the substrate(s) in hydrogen to about 1200°C, etching a few microns of silicon from the surface with a mixture of hydrogen and hydrogen chloride, depositing the required thickness of silicon, cooling the reactor and contents in hydrogen to near ambient temperature, flushing the reactor with helium or forming gas, and removing the epitaxial slices. Substrates were all oriented on a (111) plane.

Table D-I

Parameters Varied in
Deposition of Epitaxial Layers

1. Silicon Crystal Substrate
    a. Type of growth
    b. Resistivity
    c. Dislocation density
    d. Depth of damage

2. Surface Preparation of Substrate
    a. Type of polish
    b. Cleaning procedure
    c. Vapor etch

3. Growth Conditions for Epitaxial Layer
    a. Temperature
    b. Growth rate
    c. $SiCl_4$ concentration
    d. Type of reactor
    e. Dopant compound

1. Silicon Crystal Substrate

a. Type of growth. Four types of crystals were employed as substrates: pulled, Lopex*, float zone, and web.

b. Resistivity. Substrate resistivities of 0.01 and 0.1 ohm-cm as determined by standard four-point probe measurements were used for the device studies and most of the materials studies. All of these substrates were antimony doped. High resistivity (6-8 ohm-cm) boron doped, Lopex substrates were used as pilots and for certain materials studies.

c. Dislocation Density. In general, the type of crystal growth determines the dislocation density. Dislocation densities of less than 3,000 cm^{-2} and about 6,000 cm^{-2} were obtained in the pulled crystals. Lopex crystals are dislocation free. Dislocation densities of 10-30,000 cm^{-2}, and 200,000 cm^{-2} were obtained in the float zone crystals. The web crystal had a dislocation density of about 3,000 cm^{-2}.

d. Depth of Damage. Preparation of substrates for epitaxial deposition usually involves lapping the slices with progressively finer grit and then polishing either mechanically or chemically. If 1800 grit abrasive (alumina) is used for the final lapping process, all the resulting surface damage is removed in the polishing operation. In order to examine the effects of surface damage, the lapping process in some instances was stopped after lapping with 600 grit abrasive (silicon carbide). The

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* Texas Instruments Incorporated Tradename

surface was heavily damaged and a damaged region in excess of 0.001 inch deep remained after polishing in this case. The damage depth was estimated from Talysurf measurements of surface roughness and from microscopic (optical) examination of slices after etching the surface.

2. Surface Preparation of Substrate

a. Type of Polish. Both chemically and mechanically polished substrates were used. After lapping, the slices to be chemically polished were cleaned in a detergent solution. Then they were boiled, first in trichloroethylene and then in nitric acid. The slices were mounted for polishing in a teflon holder and placed in an acetic acid, nitric acid, hydrofluoric acid solution which etches at a rate of about 0.3 mil per minute at room temperature. The holder was rotated slowly during etching. After etching, the slices were quenched in water and then cleaned. The mechanically polished slices were polished to a mirror finish using successively finer polishing materials ending with $\frac{1}{2}$ micron zirconia. After polishing the substrates were 0.013 inch thick.

b. Cleaning Procedure. The standard cleaning procedure for mechanically polished slices involved cleaning in detergent solution, triple-rinsing in deionized water and light swabbing with a cotton swab saturated with acetone. The swabbing is carefully done in order to avoid scratching the polished surface. In the case of chemically polished slices, the detergent step was omitted. Some of the substrates were swabbed with acetone loaded with 100 ppm iron which had been dissolved in HCl to form a chloride. After the swabbing step, which was performed in a

Whitfield ultra clean workbench in order to reduce the possibility of dust settling on the polished surface, the substrates were kept in glass containers with ground seals until placed in the reactor for the deposition. Slices which were optically microscopically examined prior to deposition were again cleaned and swabbed before deposition. Care was taken to avoid damage to the slices as a result of handling with tweezers.

c. Vapor Etch. Standard deposition procedures call for a 3 minute vapor etch in hydrogen chloride in the reactor immediately prior to deposition. This etch removes several microns of material. It was omitted on some of the runs. The purity of the hydrogen chloride is routinely checked by means of gas chromatography. The upper limits of various impurities are shown in Table D-II. Carrier gas for the hydrogen chloride is hydrogen which has been passed through a palladium purifier. Usually a concentration of 5% hydrogen chloride is used.

3. Growth Conditions for Epitaxial Layer

a. Temperature. Three temperatures were employed: 1175°, 1225°, and 1275°C. Temperature was determined by means of an Leeds and Northrup optical pyrometer. The pyrometer readings are approximately 25°C lower than the temperatures specified.

b. Growth Rate: Three growth rates were employed: approximately 0.5, 1.5, and 3.5 microns per minute.

Table D-II Purity of Hydrogen Chloride Used for Vapor Etching of Silicon

Oxygen	$\lesssim$100 ppm
Nitrogen	$\lesssim$400 ppm
Water	$<$ 3 ppm
Carbon Dioxide	non-detectable
Organics	$<$ 1 ppm

c. $SiCl_4$ Concentration. The silicon tetrachloride concentration is governed by the growth rate chosen. Concentrations of 0.4, 0.7, and 4% were used. Hydrogen which has been passed through a palladium purifier is used as the carrier gas. The silicon tetrachloride is distilled several times before use. It is obtained as a commercial product from the Chemical Materials Department of Texas Instruments Incorporated. N-type layers with a resistivity of 50 ohm-cm can be made from undoped $SiCl_4$ in a clean reactor system.

d. Type of Reactor. Depositions were made in three types of multi-slice reactors: Horizontal, with gas flow in the direction of the slices (longitudinal); horizontal, with gas flow across the row of slices (transverse); and vertical. Photographs of the flow system employed are shown in Figs. D-1 and D-2 and a schematic diagram of the reactor system is shown in Fig. D-3.

e. Dopant Compound. Three compounds were used to dope the deposited layers: PH_3, PCl_3, and $SbCl_5$.

4. Discussion. If all these variables were permuted and combined there would be nearly 20,000 possible combinations. Accordingly the various parameters were grouped, and only 36 of the possible combinations were actually prepared. These are summarized in Table D-III.

After deposition, all layers were examined to determine if the specifications for the test device were met. Thickness was determined by an infrared reflection interference technique

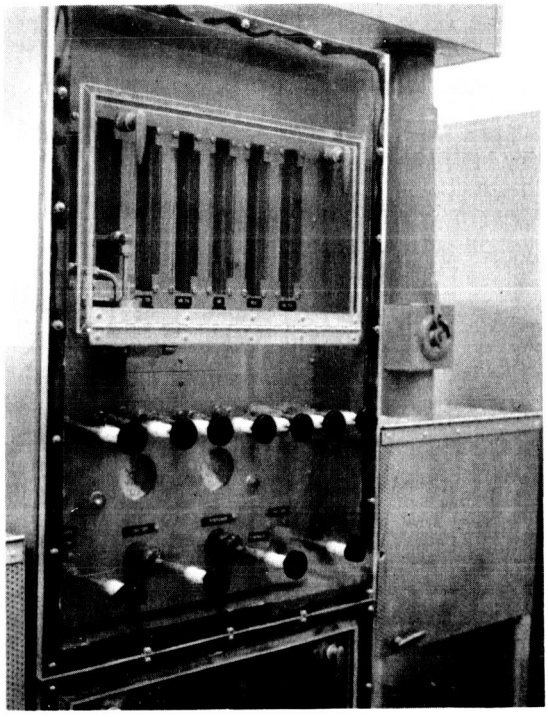

Fig. D-1 Epitaxial Control Panel and Reactor Enclosure

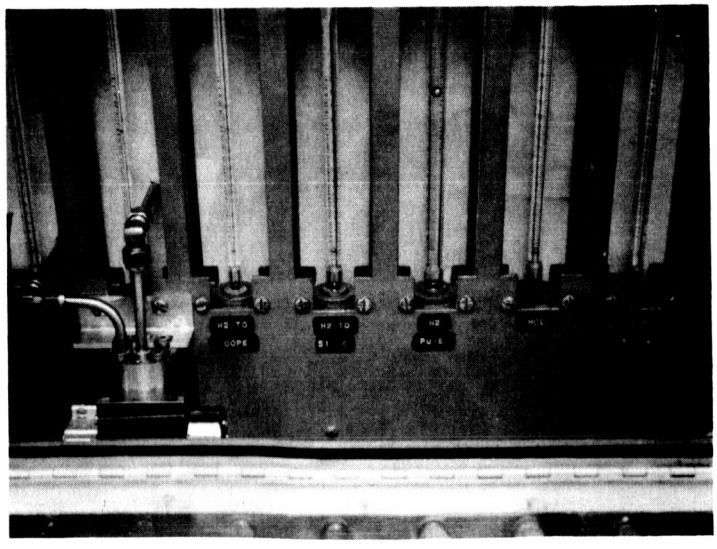

Fig. D-2 Gas Flow Metering Portion of Control Panel

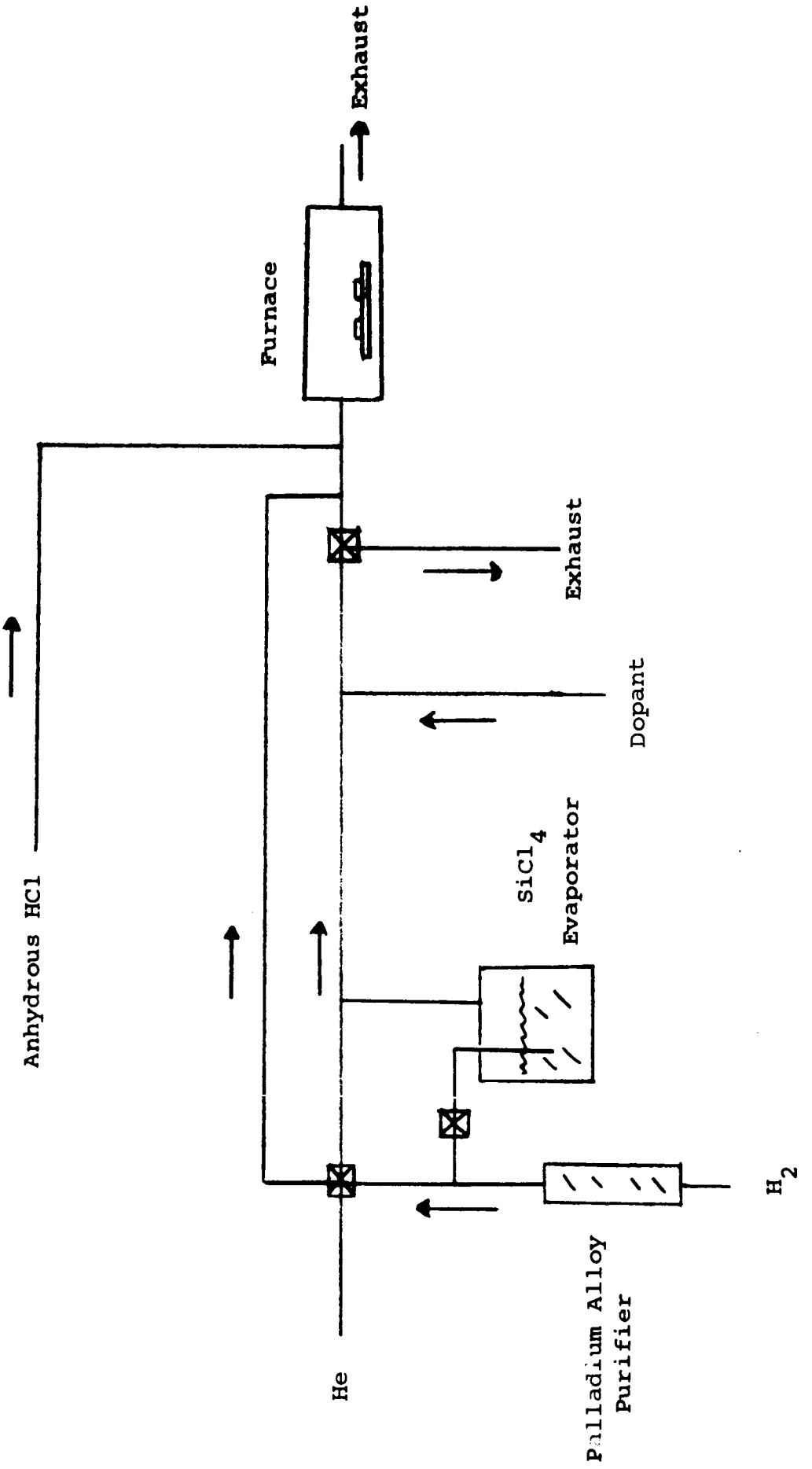

Fig. D-3 Schematic Diagram of Epitaxial Deposition System

Table D-III - Deposition Conditions

Run #	Xtal Type	Substrate ρ (Ω-cm)	Substrate Disloc Density (cm^{-2})	Surface Damage	Polish Procedure	Cleaning Procedure	In-reactor Etch	Deposition Temp (°C)	Deposition Rate (μ/min)	$SiCl_4$ Conc. (%)	Reactor Type	Doping Agent
1	Pulled	0.01	<3000	Yes	MP	Routine	Yes	1225	~ 1.5	0.7	Horiz (L)	PH_3
2	"	"	"	No	CP	"	"	"	"	"	"	"
3	"	"	"	Yes	MP	Dirty Swab	"	"	"	"	"	"
4	"	"	"	No	CP	" "	"	"	"	"	"	"
5	"	"	"	Yes	MP	Routine	No	"	"	"	"	"
6	"	"	"	No	CP	"	"	"	"	"	"	"
7	"	"	"	Yes	MP	Dirty Swab	"	"	"	"	"	"
8	"	"	"	No	CP	" "	"	"	"	"	"	"
9	"	"	"	"	"	Routine	Yes	"	~ 0.5	0.4	"	"
10	"	"	"	"	"	"	"	"	~ 3.5	4.0	"	"
11	"	"	"	"	"	"	"	1275	~ 1.5	0.7	"	"
12	"	"	"	"	"	"	"	1175	"	"	"	"
13	"	"	"	"	"	"	"	1225	"	"	"	PCl_3
14	"	"	"	"	"	"	"	"	"	"	"	$SbCl_5$
15	"	"	"	"	"	"	"	"	"	"	Horiz (T)	PH_3
16	"	"	"	"	"	"	"	~1240	~ 2.4	"	Vertical	"
17	"	0.1	"	"	"	"	"	1225	~ 1.5	"	Horiz (L)	"
18	"	0.01	~6000	"	"	"	"	"	"	"	"	"
19	Lopex	0.01	<500	"	"	"	"	"	"	"	"	"

Table D-III - Deposition Conditions (continued)

Run #	Substrate Crystal Type	Substrate ρ (Ω-cm)	Substrate Disloc Density (cm^{-2})	Surface Damage	Polish Procedure	Cleaning Procedure	In-reactor Etch	Deposition Temp (°C)	Deposition Rate (μ/min)	$SiCl_4$ Conc. (%)	Reactor Type	Doping Agent
20	Lopex	0.01	<500	No	CP	Routine	Yes	1225	~ 0.5	0.4	Horiz (L)	PH_3
21	"	"	"	"	"	"	"	"	~ 3.5	4.0	"	"
22	"	"	"	"	"	"	"	1275	~ 1.5	0.7	"	"
23	"	"	"	"	"	"	"	1175	"	"	"	"
24	"	"	"	"	"	"	"	1225	"	"	"	"
25	"	"	"	"	"	"	"	"	"	"	"	$SbCl_5$
26	"	0.1	"	"	"	"	"	"	"	"	"	PH_3
27	FZ	0.01	10-30,000	"	"	"	"	"	"	"	"	"
28	FZ	"	65,000	"	"	"	"	"	"	"	"	"
29	FZ	"	200,000	"	"	"	"	"	"	"	"	"
30	Web	0.1	~8,000	"	As rec'd	"	"	"	"	"	"	"
31	Pulled	0.01	<3,000	"	MP	"	"	"	"	"	"	"
32	"	"	"	"	"	"	No	"	"	"	"	"
33	"	"	"	"	"	Dirty Swab	Yes	"	"	"	"	"
34	"	"	"	"	"	"	No	"	"	"	"	"
37	Lopex	"	<500	"	"	Routine	Yes	"	"	"	"	"
38	"	"	"	"	"	"	"	"	"	"	"	PCl_3

Note: Runs 35, 36 and 39 were special runs with mixed conditions duplicating previous runs in most respects. These will be described in the materials measurement section.

using a Beckman IR-5A spectrophotometer or by angle lap and stain; followed by an optical interference examination using sodium light; resistivity, by means of a point-contact voltage-breakdown test set[25], a photograph of which is shown in Fig. D-4; and surface quality, by optical microscopic examination.

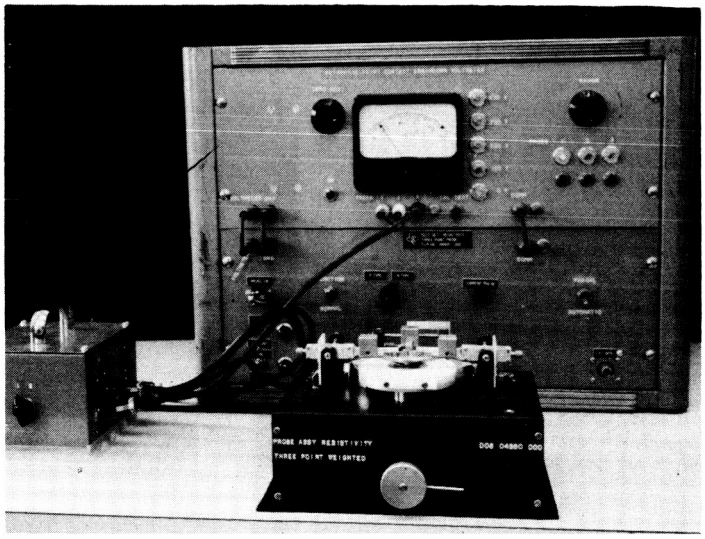

Fig. D-4 Point-Contact Voltage-Breakdown Resistivity Test Set

E. MATERIALS STUDIES

1. Surface Examination. One of the more obvious problems which might ultimately result in poor device quality is the presence of large concentrations of dislocations or stacking faults in the epitaxial film. A detailed study of films prepared according to conditions 1-8 and 31-34 was carried out in order to assess the effects of the various surface preparation procedures. Slices cut from pulled crystals with less than 3000 dislocations per cm^2 were used as the substrates.

After deposition, the slices were masked with black wax and 1/3 of the slice was etched in dislocation etch* for 2 hours while being ultrasonically agitated in order to reveal the etch pits associated with dislocations. To bring out the triangular patterns associated with stacking faults, another third of the slice was exposed to 1:3:6 etch** for one minute. These triangular patterns are also visible in the regions etched in dislocation etch.

The surface investigations showed that use of substrates with deep damaged mechanically polished surfaces resulted in epitaxial films with large concentrations of dislocations and stacking faults. If the substrate is not vapor etched in the reactor prior to deposition, large numbers of etch pits (larger than dislocations but smaller than stacking faults) are present in addition to stacking faults and dislocations. A typical slice is shown in Fig. E-1. If the substrate is vapor etched in the reactor immediately prior to deposition, these anomalous

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* 300 ml conc HNO_3, 600 ml conc HF, 2 ml Br, 23 gm $Cu(NO_3)_2$.

** 1 part HF, 3 parts HNO_3, 6 parts CH_3OOH.

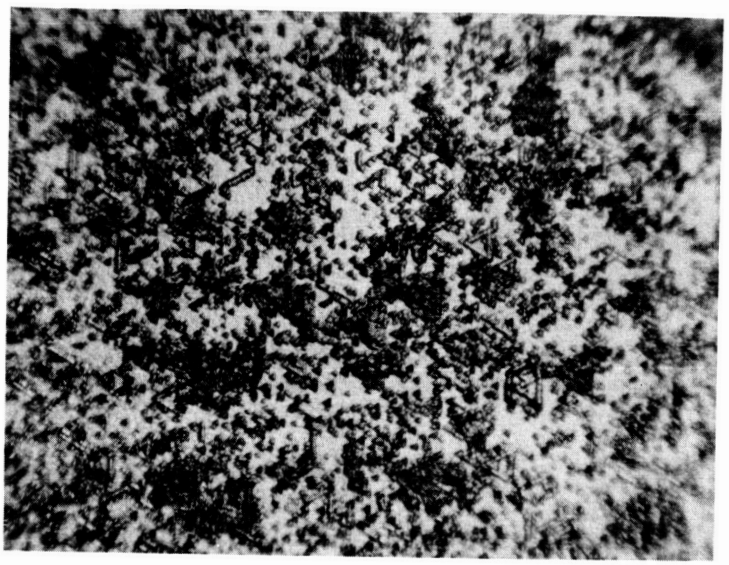

Fig. E-1 - Sample N-X-8 (Run 7). 140X. 2 hr Dislocation Etch. (not vapor etched) Stacking Faults: 2.7×10^4 cm^{-2}, Dislocations: 1.2×10^5 cm^{-2}, Anomalous pits: $>10^6$ cm^{-2}.

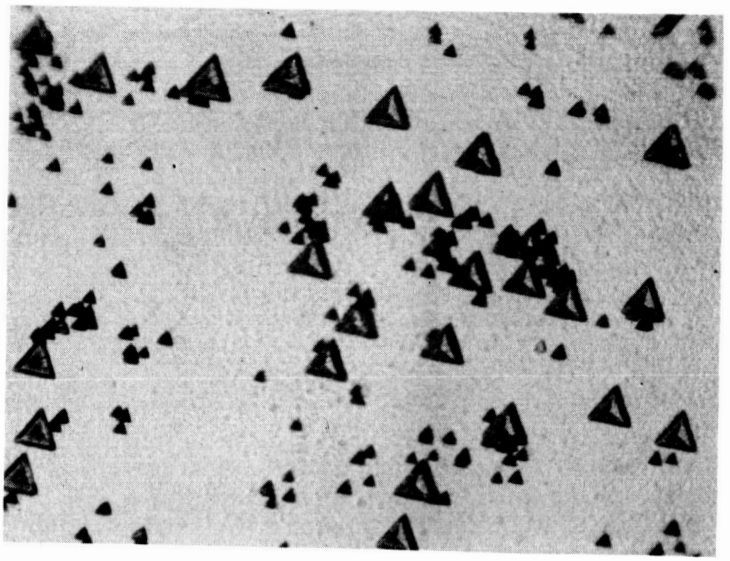

Fig. E-2 - Sample N-X-5 (Run 1). 140X. 2 hr Dislocation Etch. (vapor etched) Stacking Faults: 7×10^3 cm^{-2}, Dislocations: 4.6×10^4 cm^{-2}.

pits no longer are present and the stacking faults and dislocation densities are somewhat lower as shown in Fig. E-2. These anomalous pits may be due to groups of dislocations or to surface roughness.

Undamaged substrates, polished either chemically or mechanically, also show effects as a result of vapor etching. Typical deposits on chemically polished substrates are shown in Fig. E-3 (not vapor etched) and Fig. E-4 (vapor etched) and on mechanically polished substrates in Fig E-5 (not vapor etched) and Fig. E-6 (vapor etched). There are no anomalous etch pits of the type observed above in any case but the stacking fault density is sharply reduced by in-reactor vapor etching. No significant differences between the clean and dirty (iron contaminated) swabbing treatments were noted.

The initial studies were made on substrates cut from several pulled crystals. To ensure that the results were not distorted by this fact, a repetition of the runs employing undamaged chemically polished and mechanically polished substrates was made using one single crystal for all slices in the test. Difficulties with lattice strain were encountered in the first two crystals used and it was impossible to obtain slices free from star patterns. Slices from a third crystal were annealed carefully prior to polishing and deposition. Although evidence of strain was observed in many slices, enough strain-free slices were obtained to allow the surface examination studies to be carried out on this group. The results of the first study were confirmed by this repetition.

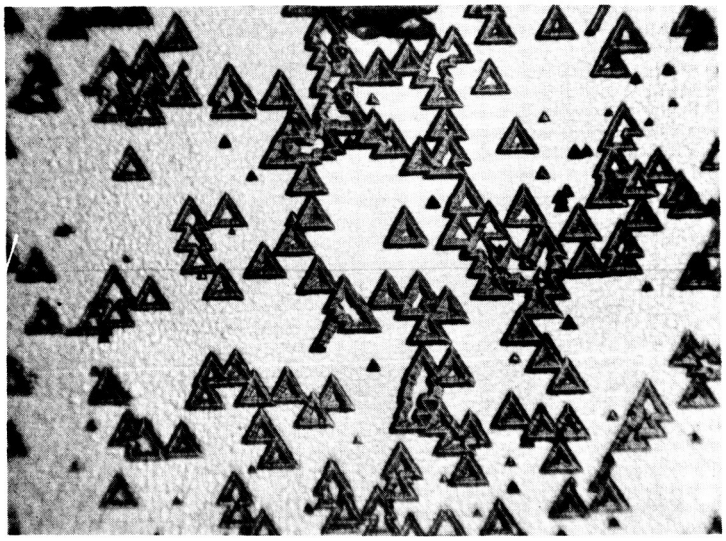

Fig. E-3 - Sample N-X-4 (Run 8). 140X. 2 hr Dislocation Etch. (not vapor etched) Stacking Faults: 2×10^4 cm^{-2}, Dislocations: 1.7×10^4 cm^{-2}.

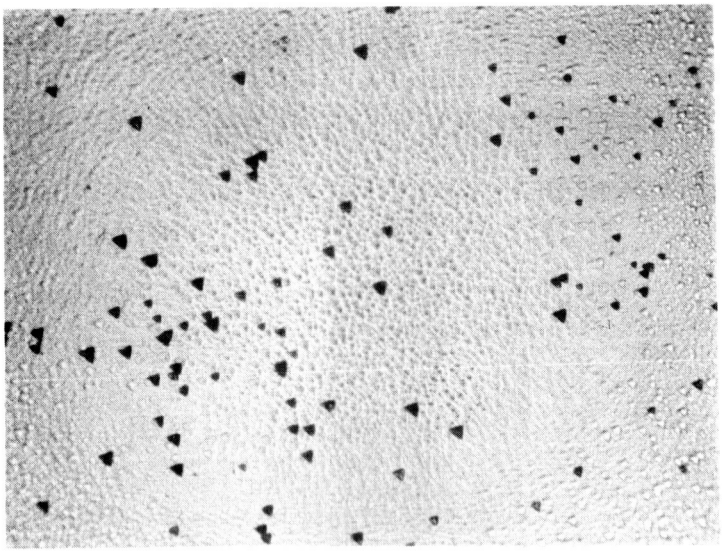

Fig. E-4 - Sample N-X-3 (Run 4). 140X. 2 hr Dislocation Etch. (vapor etched) Stacking Faults: 0, Dislocations: 2×10^4 cm^{-2}.

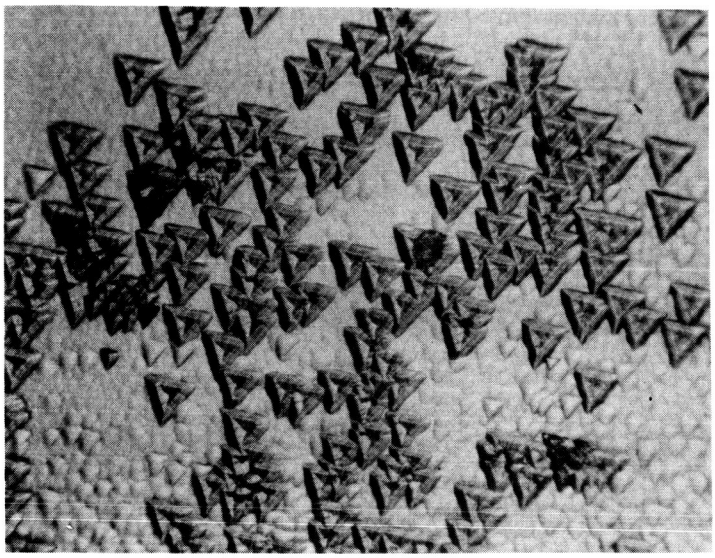

Fig. E-5 - Sample N-X-32 (Run 32). 140X. 2 hr Dislocation Etch. (not vapor etched) Stacking Faults: 4.5×10^4 cm^{-2}, Dislocations: 2×10^3 cm^{-2}.

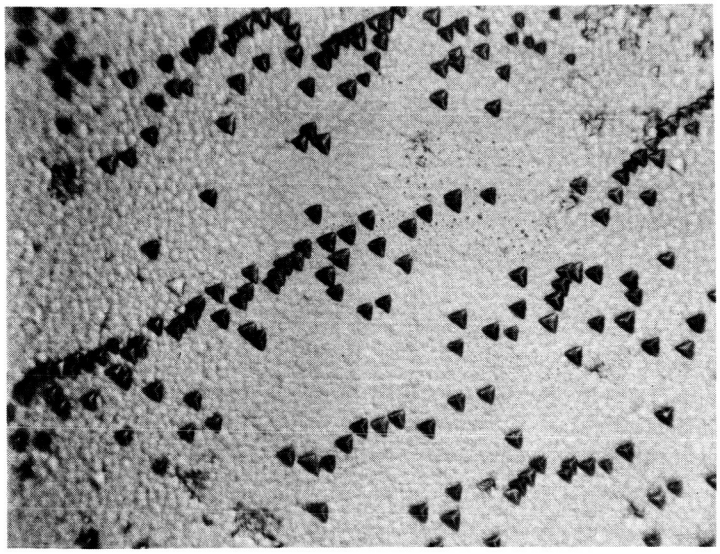

Fig. E-6 - Sample N-X-31 (Run 31). 140X. 2 hr Dislocation Etch. (vapor etched) Stacking Faults: 0, Dislocations 5.2×10^4 cm^{-2}.

In addition to these special studies, portions of each slice from which devices were made were routinely examined for etch pits and stacking faults. A strip about 1/8 inch wide next to the (110) flat was removed from the remainder of the slice by scribing and breaking. Half this strip was immersed in dislocation etch and the other half in 1:3:6 etch. The observed dislocation densities were abnormally high (generally between 10^3 and 10^5 cm^{-2}) even for films deposited on Lopex substrates. The reason for this was not understood during most of the contract period but it became clear after making the x-ray topographs described below. Since these showed that the etch pit density in the region near the flat is not typical of the rest of the slice, detailed data are not reproduced.

2. X-ray Topographic Studies. Transmission [26] and reflection x-ray topography were also employed to investigate the effect of pre-deposit surface treatments on the gross crystalline perfection of silicon epitaxial layers. X-ray topography is a non-destructive method to display photographically the intrinsic lattice flaws inherent to crystal growth.

Transmission methods have been utilized previously to record imperfections in thick slices (1-2mm) of silicon, germanium, and gallium arsenide. The distributions of defects over large surface area ($\approx$ 1 in^2) may be mapped by the employment of the scanning-reflection method[10] which was developed to study epitaxial film perfection independently of substrate effects.

The sample was mounted on a goniometer head and the film or substrate was oriented with the aid of a scintillation detector-ratemeter circuit. The instrument used was a Jerrell Ash microfocus generator. Characteristic copper radiation was employed. The effective size of the spot-focus viewed at 6 degrees was 100 microns. Nickel foil (≈0.002 in) was placed over the film holder to filter the radiation diffracted from the sample. Kodak Type A plates were utilized. The average exposure time was 2 hours.

Substrates were cut from a 0.01 ohm-cm antimony doped Lopex crystal. Prior to deposition, the substrates were chemically etched and checked for defects by means of transmission x-ray topography. No defects were observed. A typical photograph is shown in Fig. E-7. Slices were then cleaned and swabbed, using either clean acetone as in the standard procedure or acetone loaded with 100 ppm iron. Two depositions were made. In the first, the substrates were vapor etched prior to deposition while in the second they were not. The pre-deposit history of each substrate slice is summarized in Table E-I.

A (333) topograph of sample 391 is depicted in Fig. E-8. Slip-induced dislocations are observed (arrow) at the slice periphery in the region of the (110) flat ground on the ingot.* A (333) topograph of sample 392 (Fig. E-9) reveals intense slip at the sides (arrow A) and top (arrow B). Moderate slip at the top and sides of sample 393 (Fig. E-10) is also observed. The (333) topograph of sample 394 (Fig. E-11) yields surface scratches (arrow A) and slip (arrow B).

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* The (110) flat is at the top of the photograph for each sample.

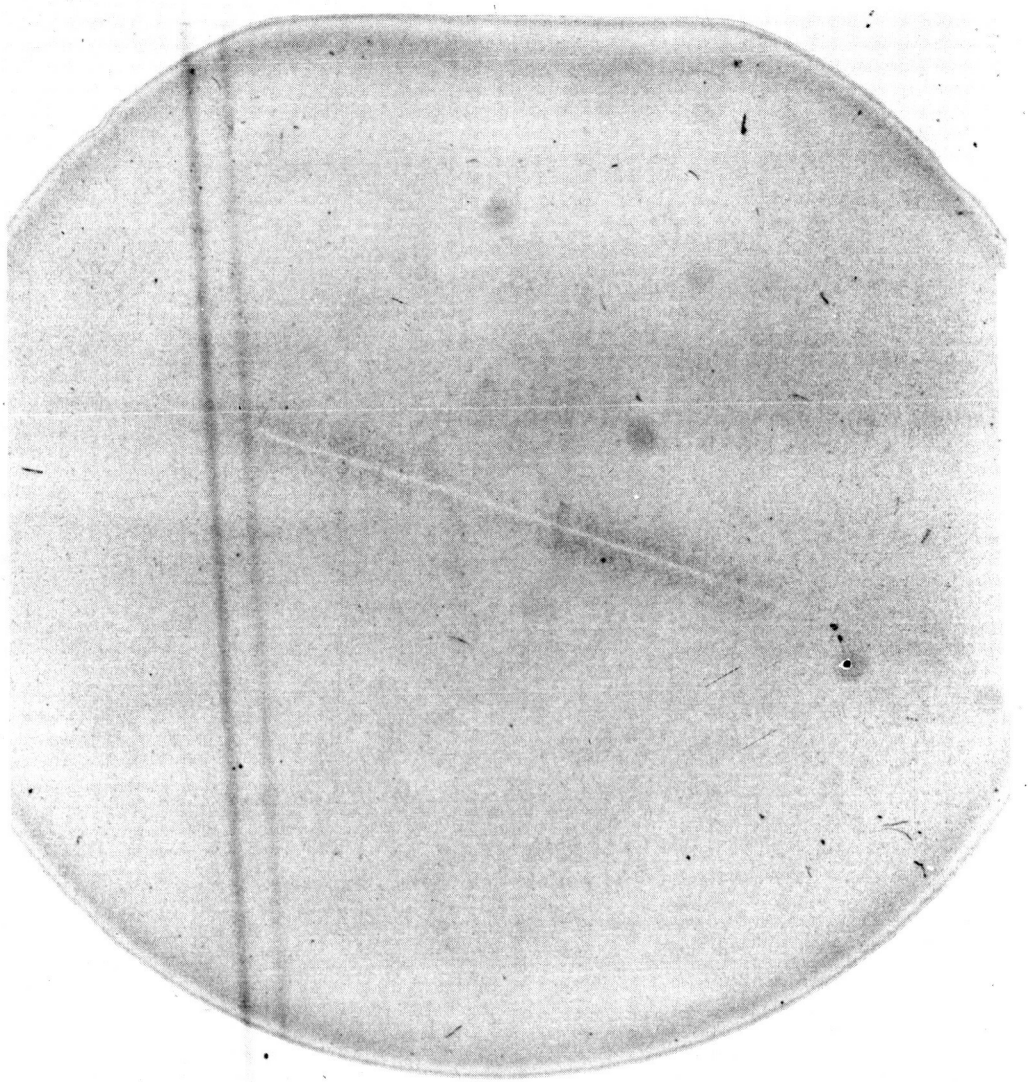


Fig. E-7 - Transmission X-ray Topograph, Slice 394 (prior to deposition).

Table E-I Substrate History and Deposit Quality

Sample	Substrate		Film			
	Swab	Vapor-etch	Topograph Shows	Etch pit count (cm^{-2}) Near Flat	At Center	Remarks
391	Clean	Yes	Moderate slip near flat	6×10^4	7×10^2	A few stacking faults near flat, none at center
392	Dirty	Yes	Heavy slip near flat	8×10^4	7×10^1	A few stacking faults near flat, none at center
393	Clean	No	Moderate slip near flat	2×10^5	3×10^2	Many stacking faults near flat, none at center
394	Dirty	No	Heavy slip near flat, scratch	2×10^5	2×10^2	Many stacking faults, scratch

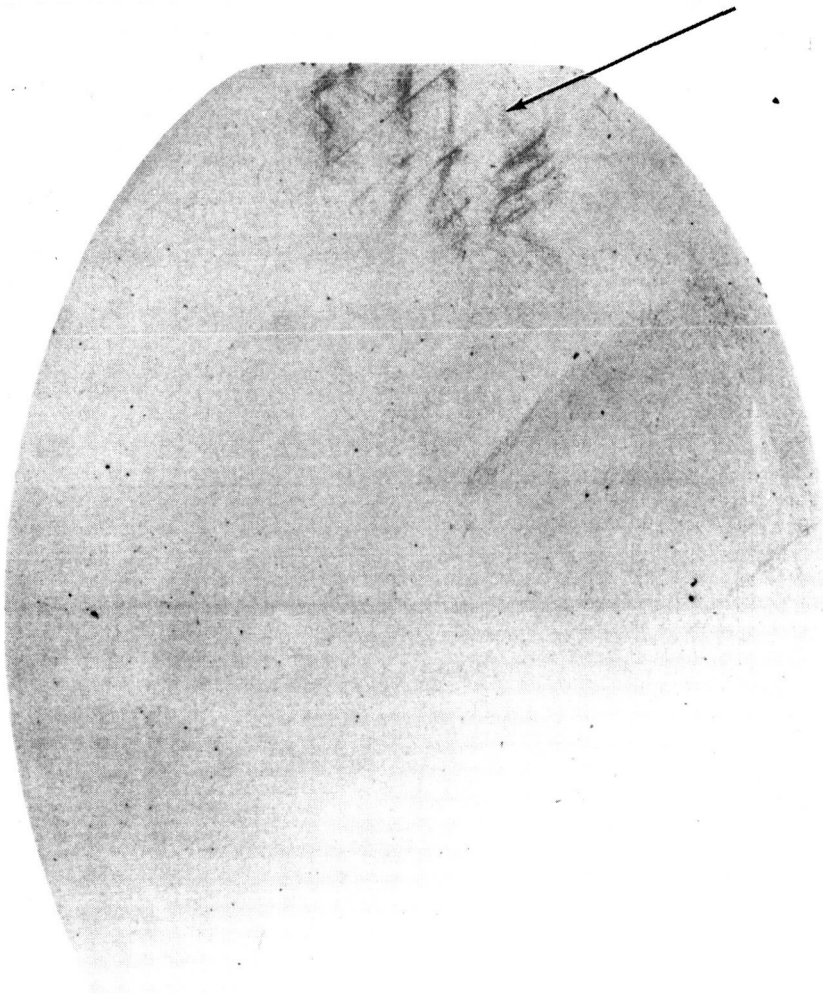


Fig. E-8 - (333) Reflection X-ray Topograph, Slice 391.

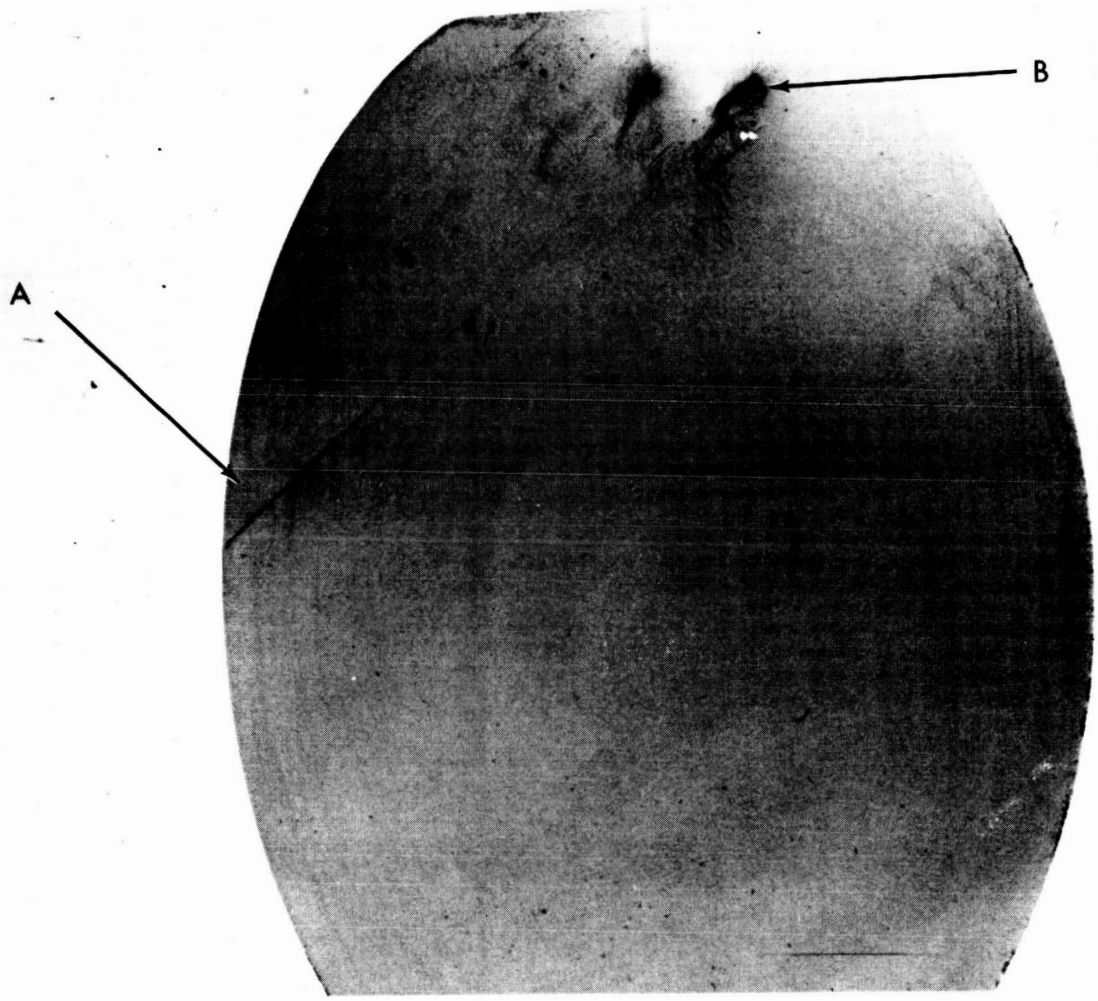


Fig. E-9 - (333) Reflection X-ray Topograph, Slice 392.

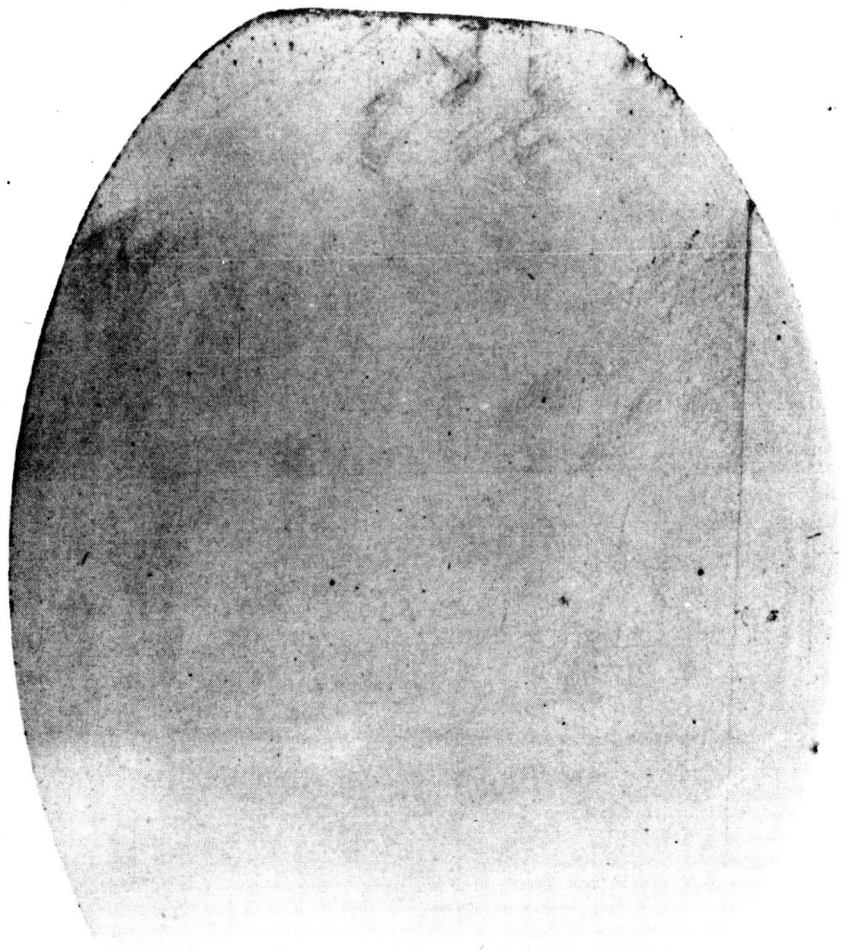


Fig. E-10 - (333) Reflection X-ray Topograph, Sample 393.

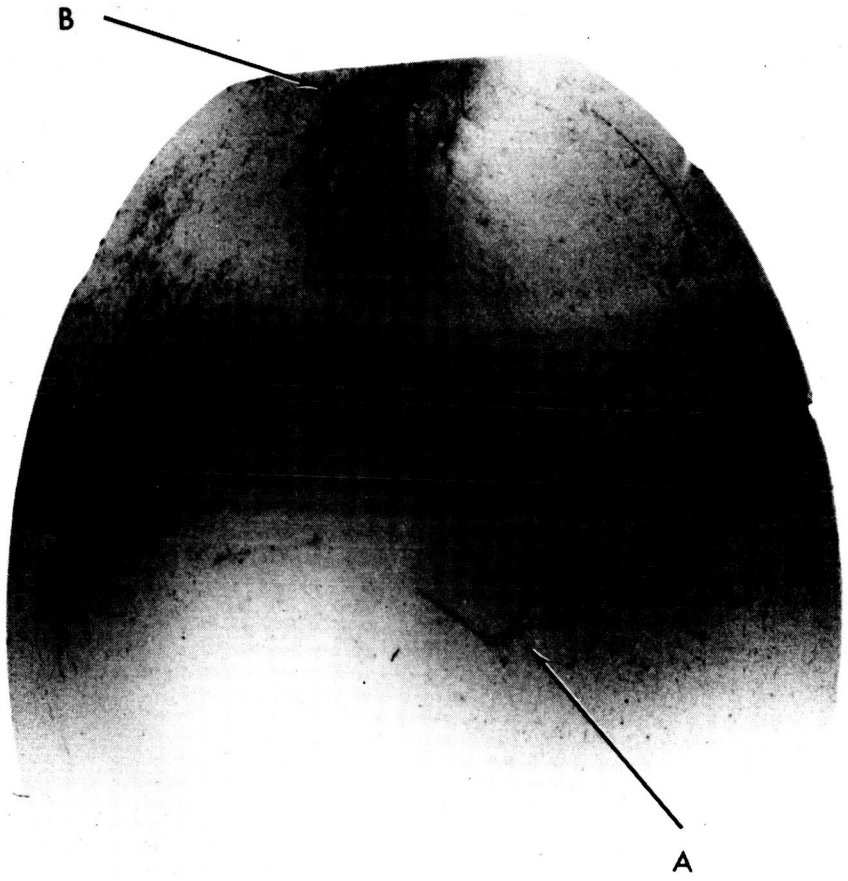


Fig. E-11 - (333) Reflection X-ray Topograph, Slice 394.

The slip at the top of the slices (in each figure) is consistent and appears to be associated with the flat. The grinding operation employed to produce the flat probably causes a strained region at the edge which propagates into the slice and the epitaxial layer during the heat cycle associated with deposition. It can be seen that the effect persists even though the substrates have been chemically etched after grinding and prior to deposition. Although the polishing etch used did not relieve the strain associated with the grinding, it is possible that a more selective etch such as NaOH would do so. The possibility that the slip is a function of the position of the slice on the susceptor cannot be ignored completely since the slices are normally placed in the reactor in the same relative orientation. Although this possibility seems unlikely further study will be required to establish the mechanism definitely.

After taking the topographs, the slices were etched in dislocation etch to bring out dislocations and stacking faults. Counts of etch pits associated with dislocations in a region near the flat and in the center of the slice are given in Table E-I. Photomicrographs from which the counts were made are shown in Figs. E-12 to E-15. It can be seen that the etch pit counts also show a marked increase near the flat.

Variations with surface preparation are much less significant than variations across the slice. However, it should be noted that the in-reactor vapor etch significantly reduces the number of stacking faults which are present. Although the topographs indicate that the films which were swabbed with acetone containing iron exhibit greater slip, this difference is not apparent in the photomicrographs.

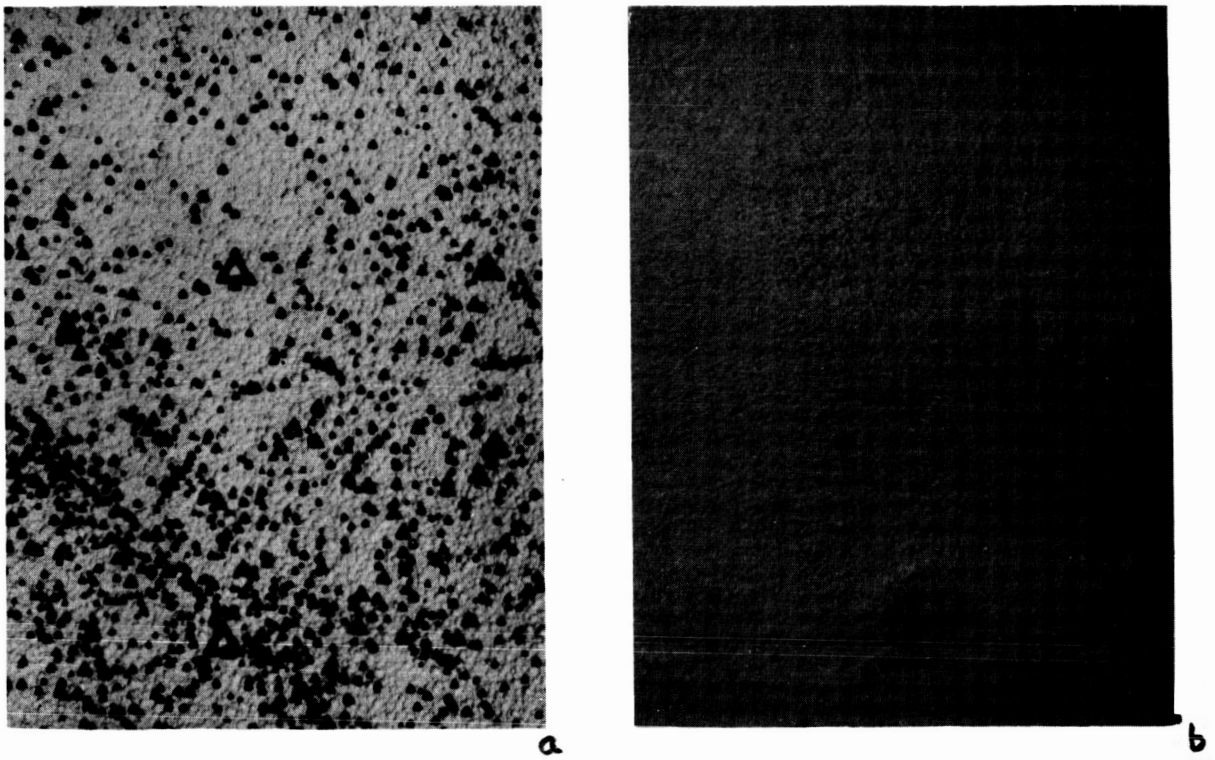


Fig. E-12 Sample 391. 70X. 2 hr. Dislocation Etch.
a) Near flat; b) Center of slice

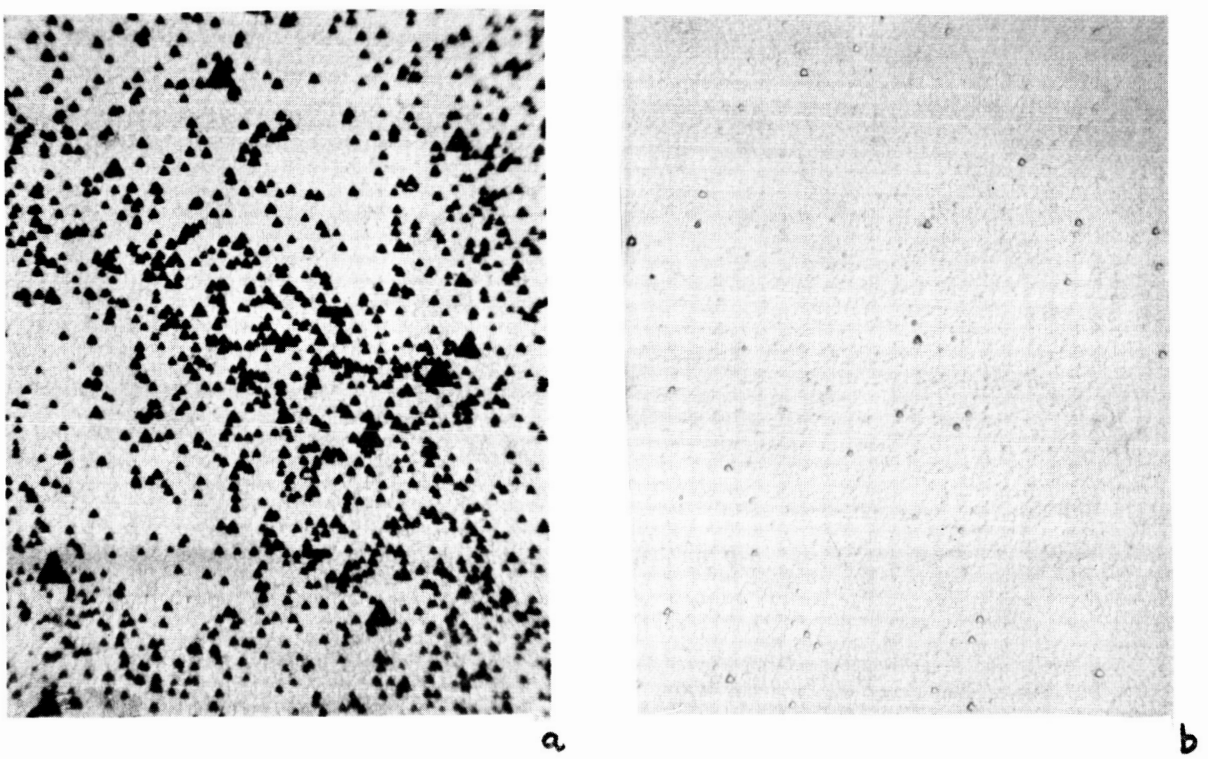


Fig. E-13 Sample 392. 70X. 2 hr. Dislocation Etch.
a) Near flat; b) Center of slice

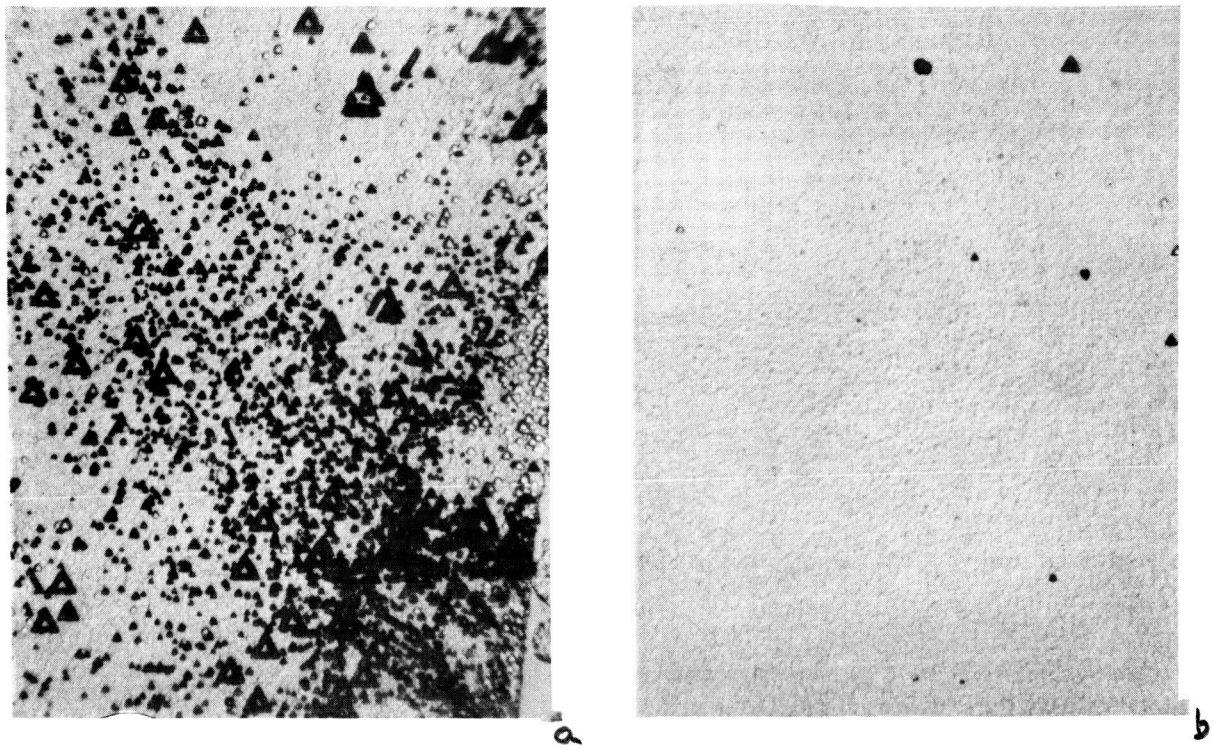


Fig. E-14 Sample 393. 70X. 2 hr. Dislocation Etch.
a) Near flat; b) Center of slice

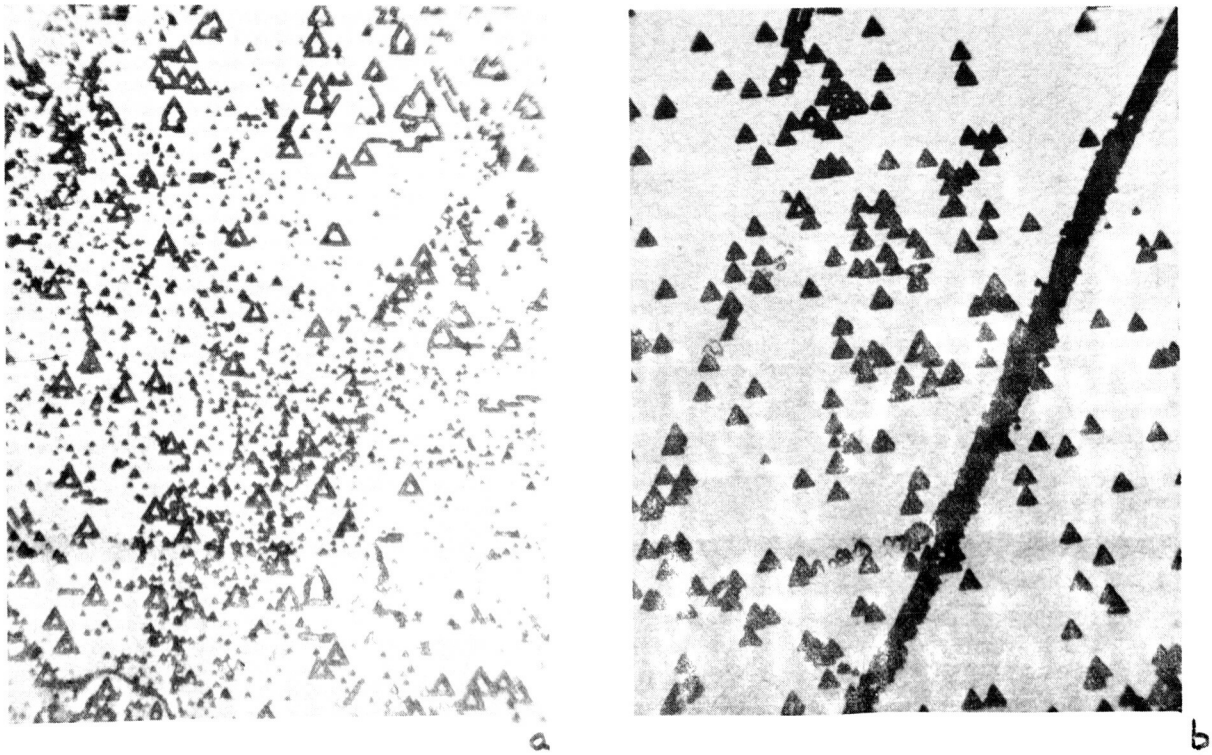


Fig. E-15 Sample 394. 70X. 2 hr. Dislocation Etch.
a) Near flat; b) Center of slice

This study was undertaken during the final phase of the contract when the technique and facilities became available. Although it appears to be very fruitful, lack of time prevented a full exploitation of it during the course of the contract effort.

3. Electrical Studies. Attempts were made to study resistivity and mobility of epitaxial films by direct measurement. Hall bar patterns were mesa etched in the films and contacts soldered to the side arms. Two measurements were to have been made on each slice. In the case of the p-type substrate, measurements could be made directly on the n-type deposit. Another part of the slice was diffused with a p-type emitter-like structure and the characteristics of the n-type deposit under the diffused layer were to be measured. In the case of the n-type substrate, the p-type layer was diffused over the entire slice. The characteristics of this layer could then be measured. An n-type emitter-like layer was diffused into a portion of the slice and the characteristics of the p-type layer under this diffused layer were to be measured.

Hall effect and resistivity measurements on a series of six n-type films deposited on p-type substrates revealed that the leakage resistance between film and substrate was the same order of magnitude as the resistance along the film. It proved impossible to improve the isolation significantly by reverse biasing the p-n junction. Consequently, the accuracy of the electrical measurements was not sufficient to draw any firm

conclusions. Because the variations in electrical properties (and, as will be seen below, in device properties) appeared not to be highly significant, the major study which would have been required to resolve the leakage difficulties was not undertaken and no further measurements were made.

F. DEVICE DESCRIPTION AND FABRICATION

The test device chosen for this contract was the 2N2432, an npn, double diffused, epitaxial planar silicon transistor. This is a high-reliability, high-speed chopper approved for use by NASA, Huntsville, under the designation SS70061. It is a 30-volt, 300-mw device with a base width of about 4 microns.

Standard 2N2432 processing techniques were used for photomasking, diffusion, device fabrication and canning operations. Details of this processing are proprietary. Four batches of devices were fabricated. The deposition runs included in each of these batches are shown in Table F-I. In general, six slices from each deposition run were started through the process. Since all 48-54 slices could not be accommodated in a diffusion run, three slices from each deposition run were included in each of two diffusion runs required for each batch of devices. Fifty or more devices were made from each slice which survived the diffusion and scribing operations.

It proved to be impossible to process the slices from deposition run 30 (web material). These slices were much thinner and much smaller than the standard slices. As a result they could not be held on the KMER spinners with the jigs and fixtures which were available.

No post-fabrication testing was employed. However all devices which were used in subsequent tests were checked for transistor action. Yields on some slices, particularly those with heavily damaged substrate surfaces, were abnormally low.

Table F-I - Device Fabrication Batches

Fabrication Batch	Epitaxial Deposition Runs
I	1, 2, 3, 4, 5, 6, 7, 8
II	9, 10, 11, 12, 13, 14, 15, 16
III	19, 20, 21, 22, 23, 24, 25, 37, 38
IV	17, 18, 26, 27, 28, 29, 30, 31, 2

G. POWER STEP-STRESS TESTS

1. Test Conditions. In order to assess the effect of variation of materials and deposition parameters on the reliability of a silicon epitaxial transistor, devices from most of the epitaxial deposition runs were subjected to a power step stress test. All epitaxial runs from which 2N2432 transistors were made were represented with the exception of runs 27 and 28 which were inadvertantly omitted. In addition, a group of 2N2432 transistors was taken off the shelf and tested in the same fashion (Run 0).

Forty devices from each group were operated at power levels of 300mw (rated power), 600mw, and 800mw. An applied voltage of 30 volts was used during the 48 hour stress period at each power level. Measurements of BV_{CEO}, I_{CBO}, I_{EBO}, h_{FE} and h_{FE}(inverse) were taken before and after each stress period. Data sheet conditions were used for these tests. These conditions are summarized in Table G-I.

2. Analysis. If a particular time interval is chosen, and units are subjected to successively greater stresses (usually temperature or temperature plus applied voltage) it is generally observed that a graph of 1/T°K versus cumulative failures is composed of straight line segments. The choice of a failure point will change the location of the curve but usually does not change the slope.

As was mentioned earlier, data were taken at power dissipation levels of 300, 600, and 800mw. In order to make curves of the kind discussed above, the junction temperature at each level must be determined. Very approximate values of

Table G-I - Test Conditions for Parameters Studied in the Power Step-stress Tests

Parameter	Test Conditions	Specifications
BV_{CEO}	I_C = 10 ma, I_B = 0	≥30 Volts
I_{CBO}	V_{CB} = 25 V, I_E = 0	≤10 na
I_{EBO}	V_{EB} = 15 V, I_C = 0	≤ 2 na
h_{FE}	V_{CE} = 5 V, I_C = 1 ma	≥ 50
$h_{FE(INV)}$	V_{EC} = 5 V, I_E = 0.2 ma	≥ 2

the junction temperature were obtained in the following manner: First, the case temperature for a device was measured as a function of power using an iron-constantan thermocouple welded to the outside of the can. This gave the results shown in Table G-II. Second, the thermal resistance between the device and the header was measured by alternately pulsing the device and measuring the wafer temperature by the forward voltage drop of the emitter-base diode. This thermal resistance varies considerably from device to device as can be seen from data taken on 12 random samples shown in Table G-III. However, no variation which could be attributed to variations in epitaxial deposition parameters was found. Third, from a combination of these, values of junction temperature at various power levels were computed according to the relationship: $T_J = T_C + \theta P$, where T_J is the junction temperature, T_C is the case temperature, θ is the average thermal resistance, and P is the power dissipated. The lower dotted line in Fig. G-1 depicts this computed junction temperature.

Other data, listed as "typical" for this device, give the two circles. These two points, coupled with the knowledge that catastrophic failure would occur above the gold-silicon eutectic (370°C) give the upper dotted curve. The difference between the two is probably due to the environment of the case. For example, the 214°C/watt case temperature increase was based on a single unit in still, unconfined air. A large number of units closely packed with poor circulation would have a greater temperature rise. It appears then that these two curves represent the extremes in temperature excursion to be expected. Accordingly the solid line was drawn to give an average number for use in plotting the data.

Table G-II - Case Temperature at Various Input Power Levels (2N2432)

Power Input	Case Temp
300mw	90°C
600mw	165°C
800mw	196°C

Table G-III - Thermal Resistance on 12 Units (2N2432)

Unit	°C/watt	
1	56	
2	14	(omitted from average)
3	64	
4	62	
5	67	
6	72	
7	55	
8	56	
9	79	
10	92	
11	62	
12	71	
Av	67	

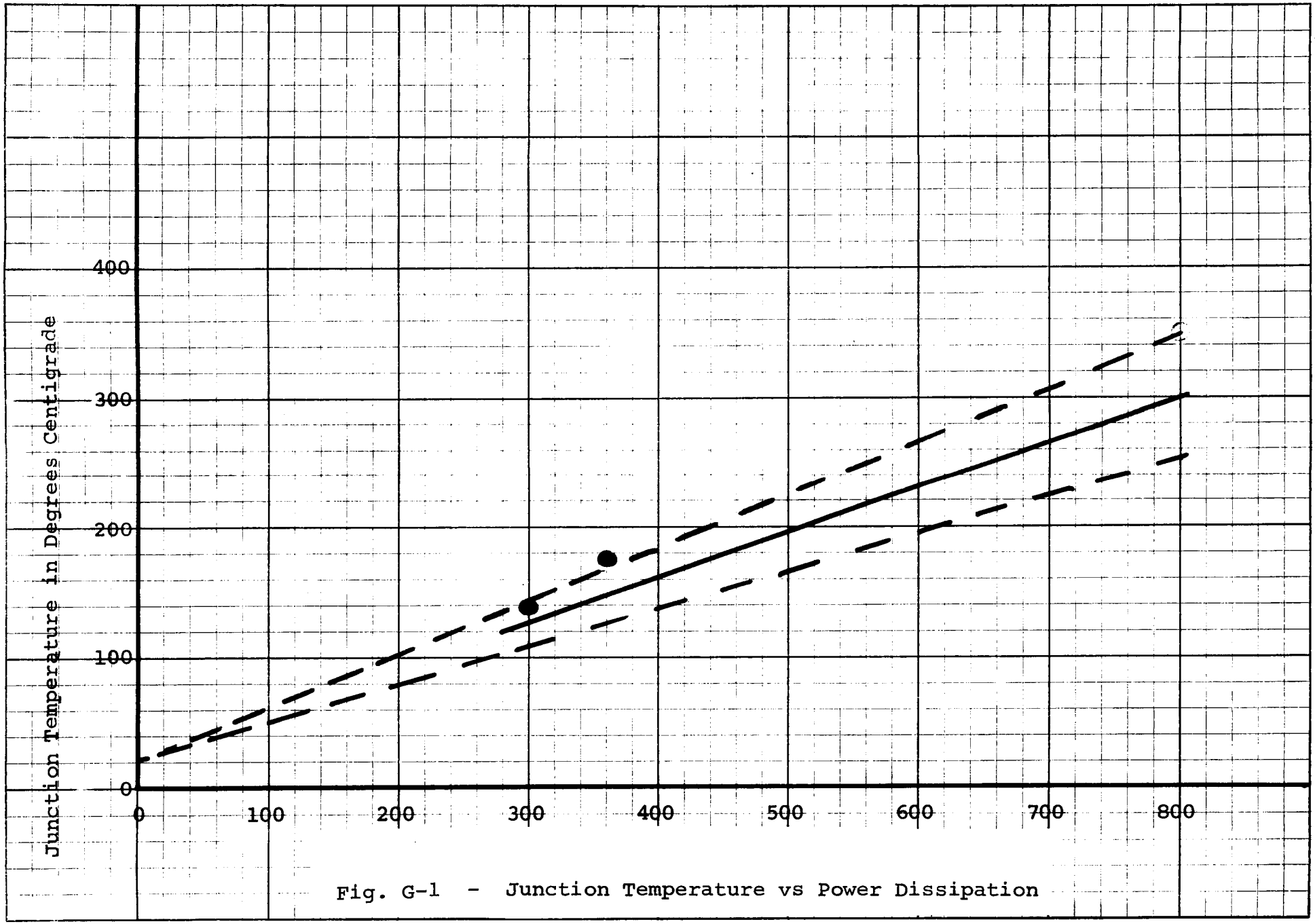


Fig. G-1 - Junction Temperature vs Power Dissipation

Table G-IV gives the per cent cumulative h_{FE} failures for the different runs and Table G-V gives similar data for I_{CBO}. As a matter of definition, an h_{FE} failure occurred when h_{FE} changed by 20%, and an I_{CBO} failure occurred when I_{CBO} increased by a factor of ten. Catastrophic failures, which will be discussed below, were not included in this analysis.

The problem now arises of how to compare the data in order to delineate any significant differences between devices constructed in the various manners. Figures G-2 through G-4 are $1/T_J$ versus cumulative h_{FE} failure plots. The junction temperature is assumed to be that of the solid line in Fig. G-1. The data are plotted on three figures in order to minimize overlap. If we assume that there are no more than three straight line segments which should pass through the three temperature points, the slopes of the segments can vary rather widely as illustrated in Fig. G-5a. It is, however, impossible for the slope of any segment to become negative, for segment 1 to have a slope less than that drawn, or for segment 2 to have a slope greater than drawn. Thus the correct lines lie in the cross-hatched regions of Fig. G-5b.

Tables G-VI and G-VII list total per cent h_{FE} and I_{CBO} failures in decreasing rank. No pattern is discernable and no conclusive interpretation of the data is possible. It should be emphasized however that "random" surface variations and differences in fabrication appear to have a greater effect on reliability than any variations in deposition conditions which have been studied thus far.

Table G-IV - Per Cent Cumulative Failures (h_{FE})

Run #	300mw	600mw	800mw
0	28	43	51
1	20	40	40
2	37	65	72
2-R	13	13	49
3	22	42	65
4	23	28	41
5	37	55	60
6	25	47	67
7	12	28	35
8	15	30	33
9	2	5	12
10	8	18	20
11	8	13	20
12	20	27	32
13	8	20	30
14	5	10	10
15	10	15	30
16	15	17	30
17	63	67	87
18	50	50	69
19	10	22	28
20	30	42	49
21	32	37	42
22	5	12	45
23	32	45	60
24	17	32	55
25	12	27	45
26	5	15	45
29	10	15	37
31	18	18	47
37	17	42	42
38	8	37	55

Table G-V - Per Cent Cumulative Failures (I_{CBO})

Run #	300mw	600mw	800mw
0	0	55	57
1	2	7	7
2	0	10	32
2-R	2	5	45
3	22	45	57
4	5	7	22
5	15	30	40
6	7	15	31
7	27	40	50
8	5	7	12
9	0	0	5
10	0	2	7
11	0	2	5
12	2	5	5
13	2	5	7
14	2	7	10
15	10	20	27
16	2	2	2
17	3	11	71
18	0	3	31
19	2	2	5
20	0	0	0
21	0	5	10
22	0	0	2
23	0	2	5
24	0	0	0
25	7	7	7
26	2	10	22
29	0	5	35
31	2	5	32
37	0	0	0
38	0	2	2

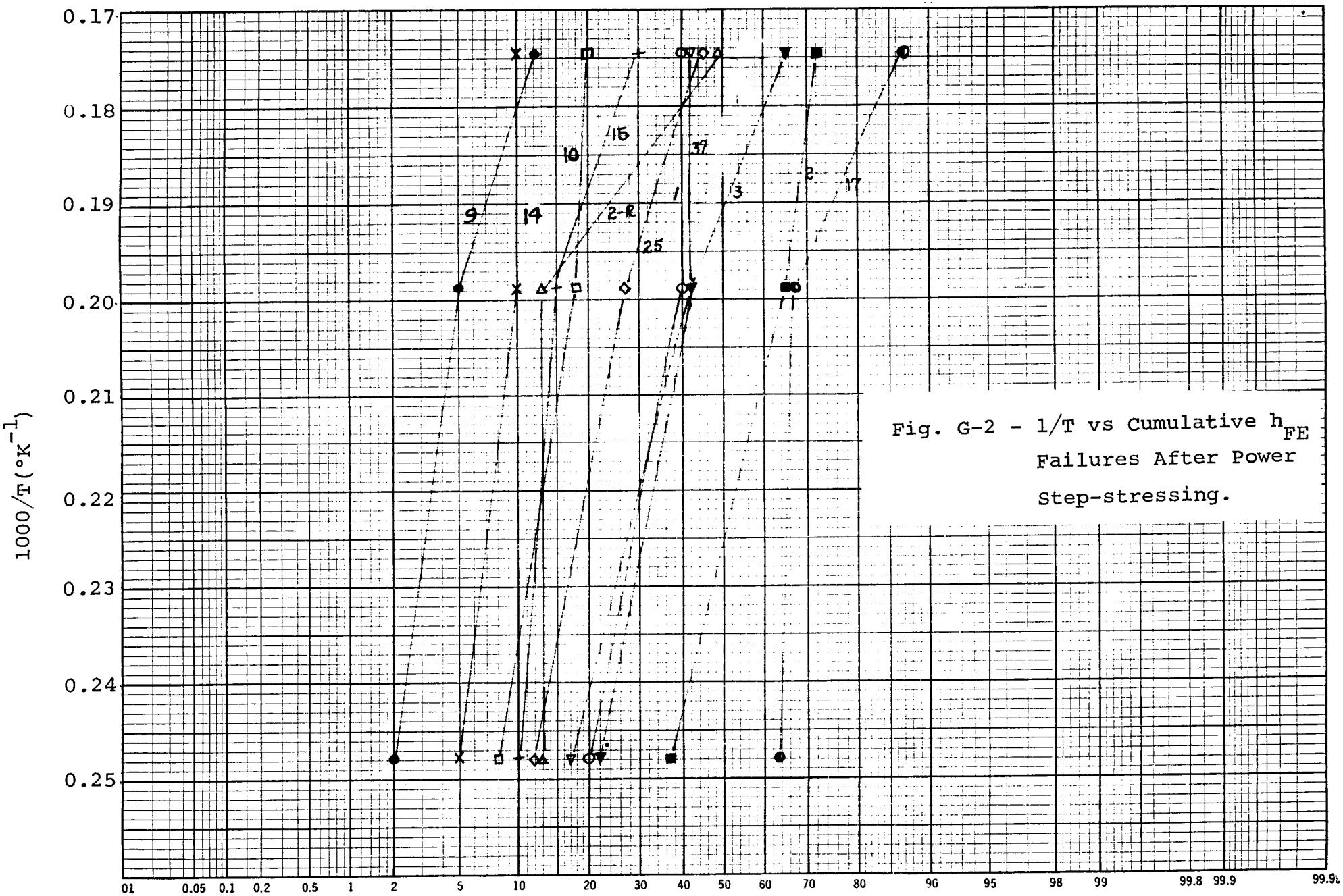


Fig. G-2 - 1/T vs Cumulative h_{FE} Failures After Power Step-stressing.

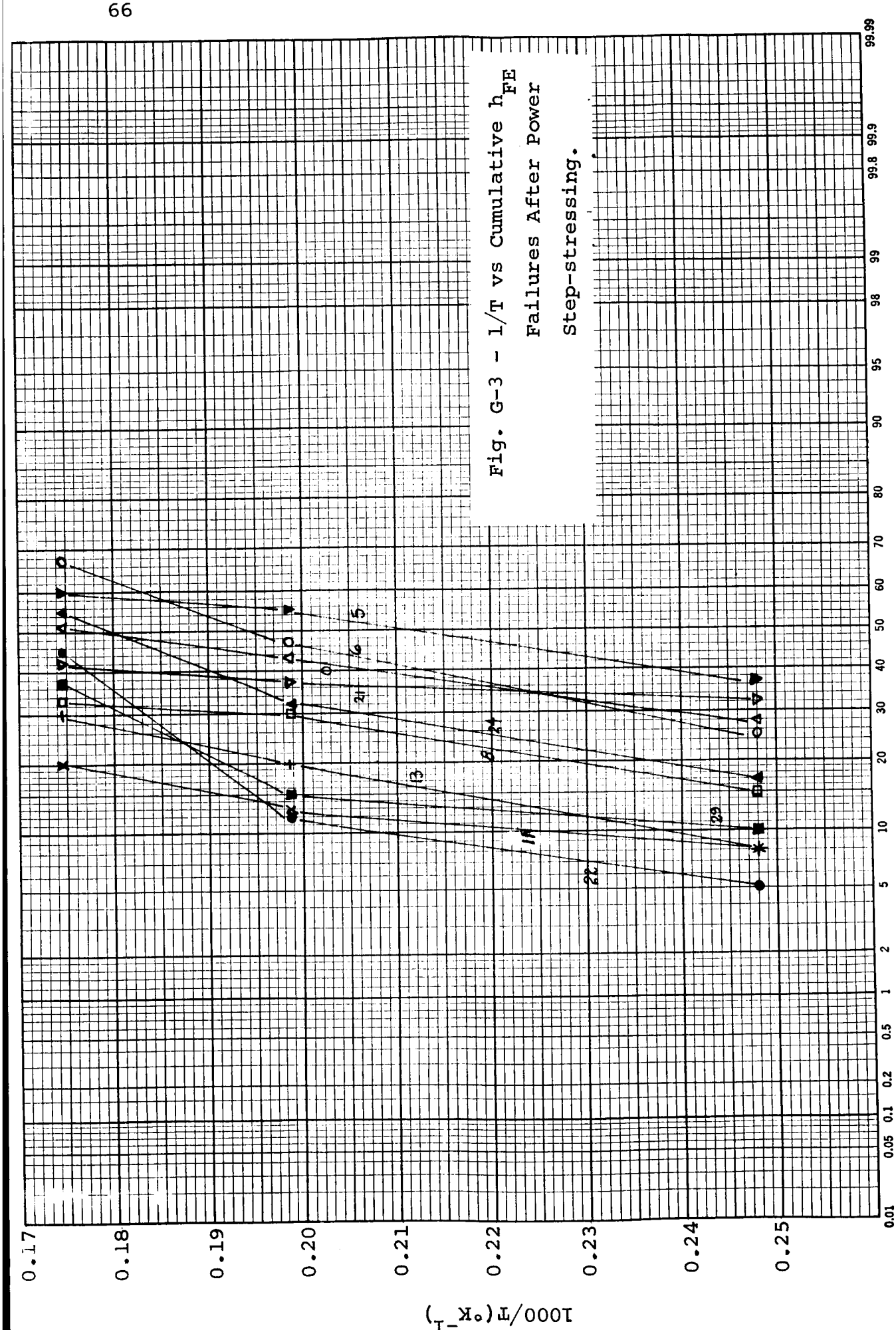


Fig. G-3 - 1/T vs Cumulative h_{FE} Failures After Power Step-stressing.
1000/T(°K⁻¹)
0.17
0.18
0.19
0.20
0.21
0.22
0.23
0.24
0.25
% Cumulative h_{FE} Failures
99.99
99.9
99.8
99
98
95
90
80
70
60
50
40
30
20
10
5
2
1
0.5
0.2
0.1
0.05
0.01

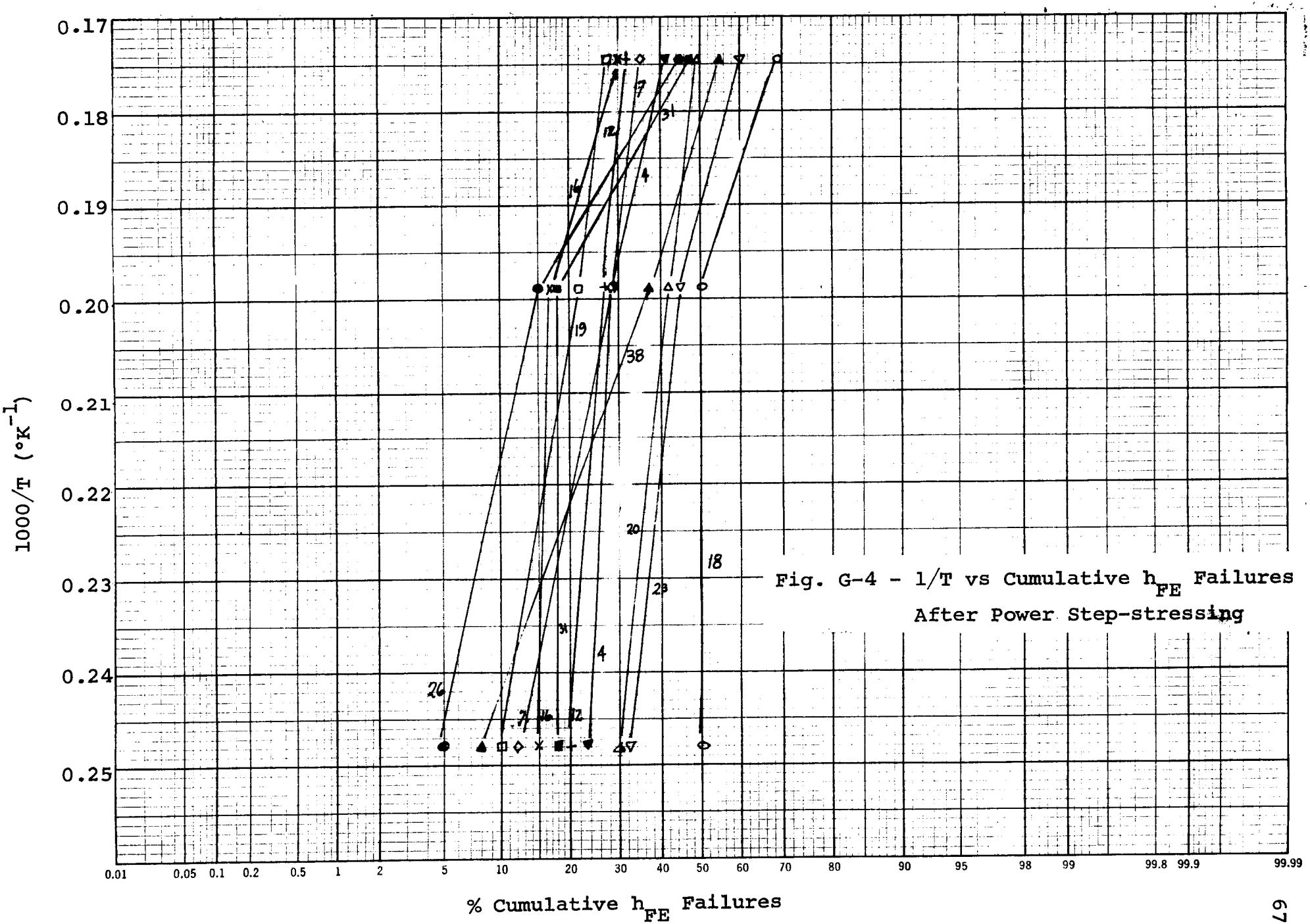


Fig. G-4 - 1/T vs Cumulative h_{FE} Failures After Power Step-stressing

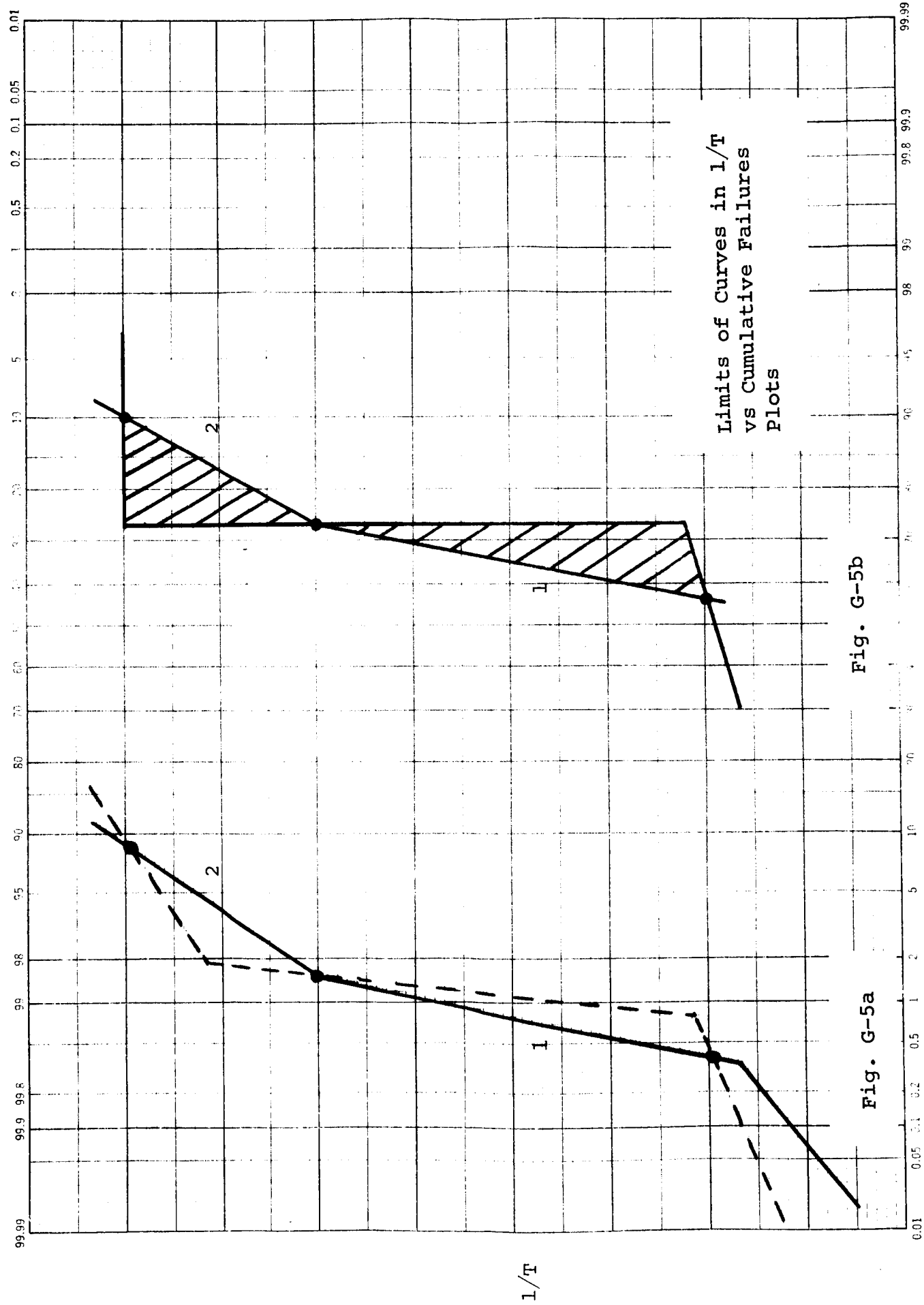

Limits of Curves in 1/T
vs Cumulative Failures
Plots
Fig. G-5b
Fig. G-5a
1
2
1
2
1/T
% Cumulative Failures

Table G-VI - Total Per Cent Failures (h_{FE})

Run No.	Total Per Cent Failure
17	87
2	72
18	69
6	67
3	65
5	60
*23	60
*24	55
*38	55
0	51
*20	49
2-R	49
31	47
*26	45
22	45
*25	45
*21	42
*37	42
4	41
1	40
29	37
7	35
8	33
12	32
15	30
16	30
13	30
*19	28
10	20
11	20
9	12
14	10

* Lopex Substrate

Table G-VII - Total Per Cent Failures (I_{CBO})

Run No.	Total Per Cent Failure
17	71
0	57
3	57
7	50
2-R	45
5	40
29	35
2	32
31	32
18	31
6	31
15	27
26	22
4	22
8	12
14	10
*21	10
1	7
10	7
*25	7
13	7
11	5
9	5
12	5
*19	5
*23	5
30	2
16	2
*22	2
*24	0
*20	0
*37	0

* Lopex Substrate

This conclusion is also substantiated by a detailed examination of the means of the values of the various parameters studied, the means of the values of the parameters after stressing normalized to their initial value and standard deviations of the various parameters. There were no obvious differences in any of these indices which could be attributed to differences in preparation of the epitaxial layers.

3. Catastrophic Failures. Many devices failed catastrophically during the course of the step-stress tests. The number which failed the h_{FE} test are listed in Table G-VIII. Many of the failed devices were sectioned in order to determine the cause of failure. In every case examined, gold from the emitter or base lead alloyed across one or both junctions causing shorts. In some cases, this alloying was accompanied by melting of the emitter or base leads resulting in an external open.

Three runs (2, 7 and 19) were operated an additional 72 hours at 800 mw. The number of catastrophic failures increased sharply; characteristics of the remaining measurable units became very soft and indeterminate.

The precise cause of the alloying is not clear. It is apparent that the temperature has exceeded the gold-silicon eutectic temperature or the melting point of a gold-silicon-X alloy where X is an unknown impurity. Some evidence has been obtained which associates material imperfections such as tetrahedral growths, stacking faults, or dislocations with these failures. For example, a break in the collector-base junction (such as the one in Fig. G-6)

Table G-VIII - Catastrophic Failures (h_{FE})

Run #	Cumulative Failures After			
	300mw	600mw	800mw	Batch
0	1	2	2	-
1	0	0	0	I
2	0	3	5	I
2-R	1	2	17	IV
3	0	3	9	I
4	1	1	4	I
5	0	3	9	I
6	0	3	4	I
7	0	3	4	I
8	0	1	1	I
9	0	0	0	II
10	1	3	4	II
11	0	0	0	II
12	0	0	1	II
13	0	0	0	II
14	0	0	0	II
15	0	0	2	II
16	0	0	1	II
17	2	3	27	IV
18	4	4	15	IV
19	0	1	1	III
20	0	0	0	III
21	0	1	2	III
22	0	0	0	III
23	0	1	1	III
24	0	1	1	III
25	0	0	0	III
26	0	0	8	IV
29	0	0	9	IV
31	2	2	10	IV
37	0	0	0	III
38	0	1	1	III

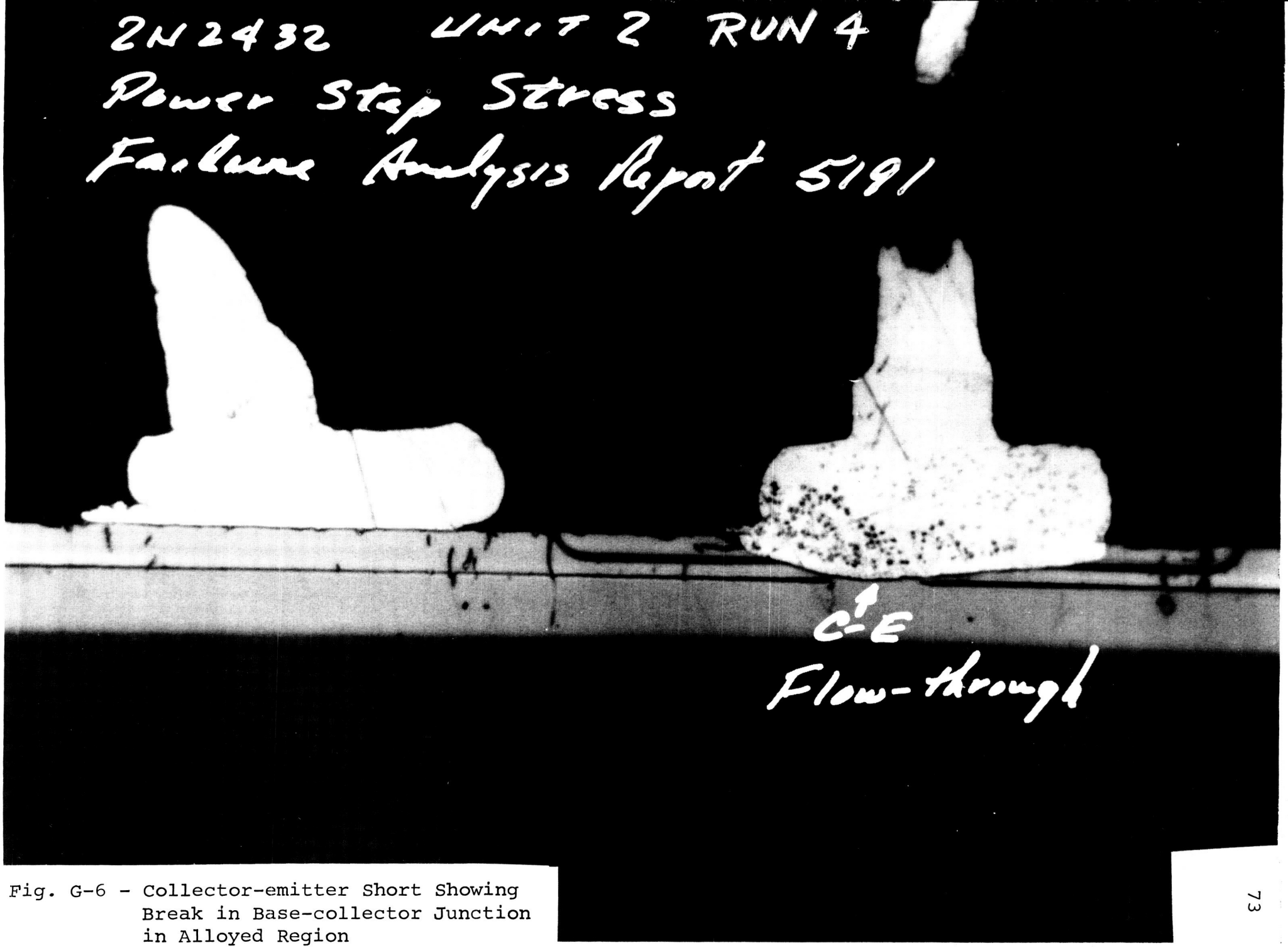


Fig. G-6 - Collector-emitter Short Showing Break in Base-collector Junction in Alloyed Region

in the region of the gold penetration is highly suggestive that one or more of these may be present in the failed units. Also, the low incidence of catastrophic failure among devices made from layers which were deposited on Lopex substrates with their significantly lower defect density suggests that this may be the case. In devices of this type which did fail the break is apparently absent as shown in Figs. G-7 and G-8.

On the other hand, devices made from layers which were deposited on the high dislocation density float-zone substrates showed no abnormal number of catastrophic failures. There is a suggestion that uncontrolled processing variations between batches might be significant. The wide spread in thermal resistance values from device to device which was noted in Table G-III probably results from variation of thermal conduction across the wafer-header contact and it seems possible that this is the most significant quantity. Variations in collector resistance may also be significant. It should also be noted that leads on top of tetrahedral growths do not always alloy through. An example is given in Fig. G-9.

Further study in this area will be required in order to resolve the question fully.

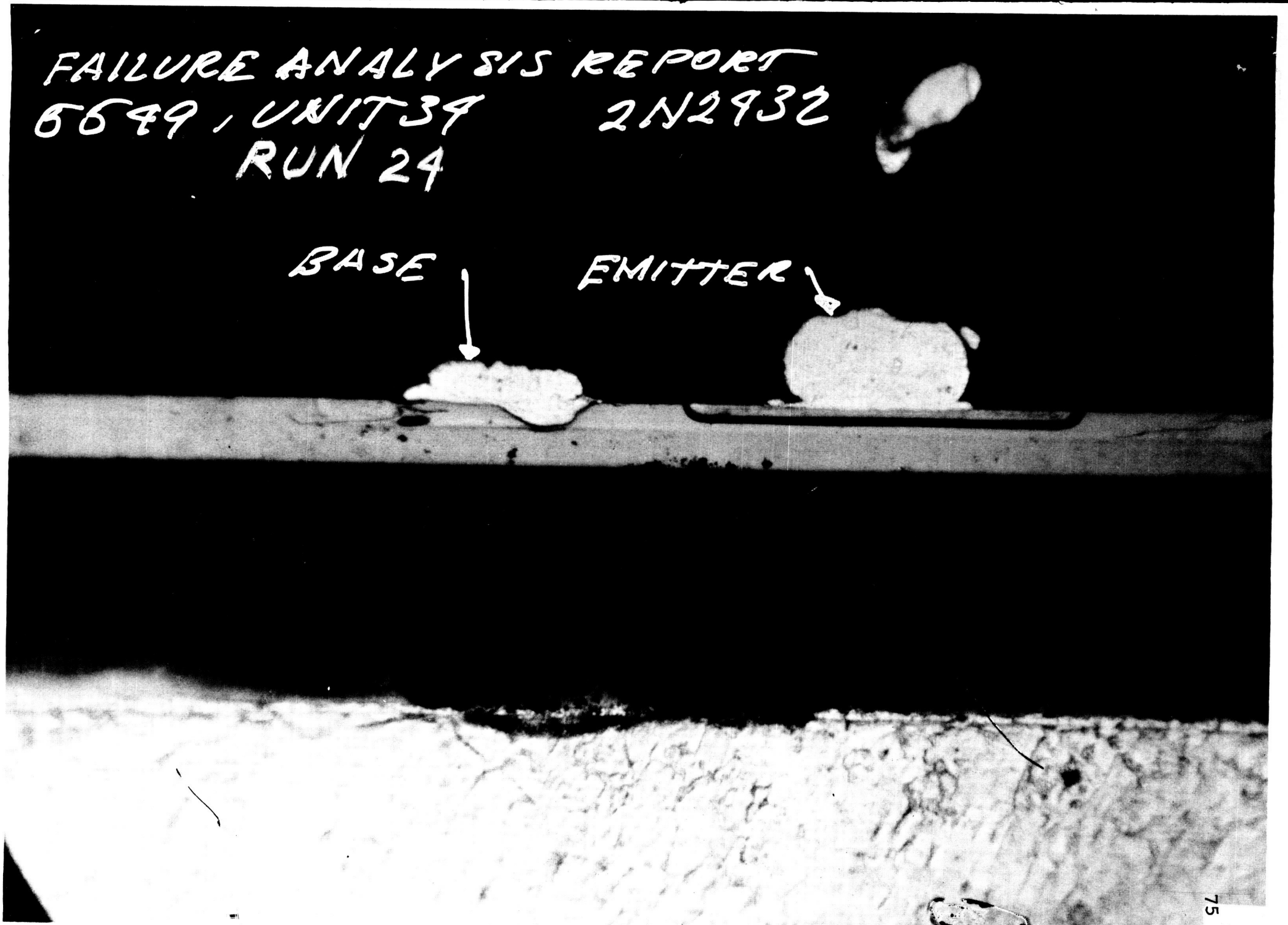


Fig. G-7 - Base Collector Short

Fig. G-8 - Emitter Base Short

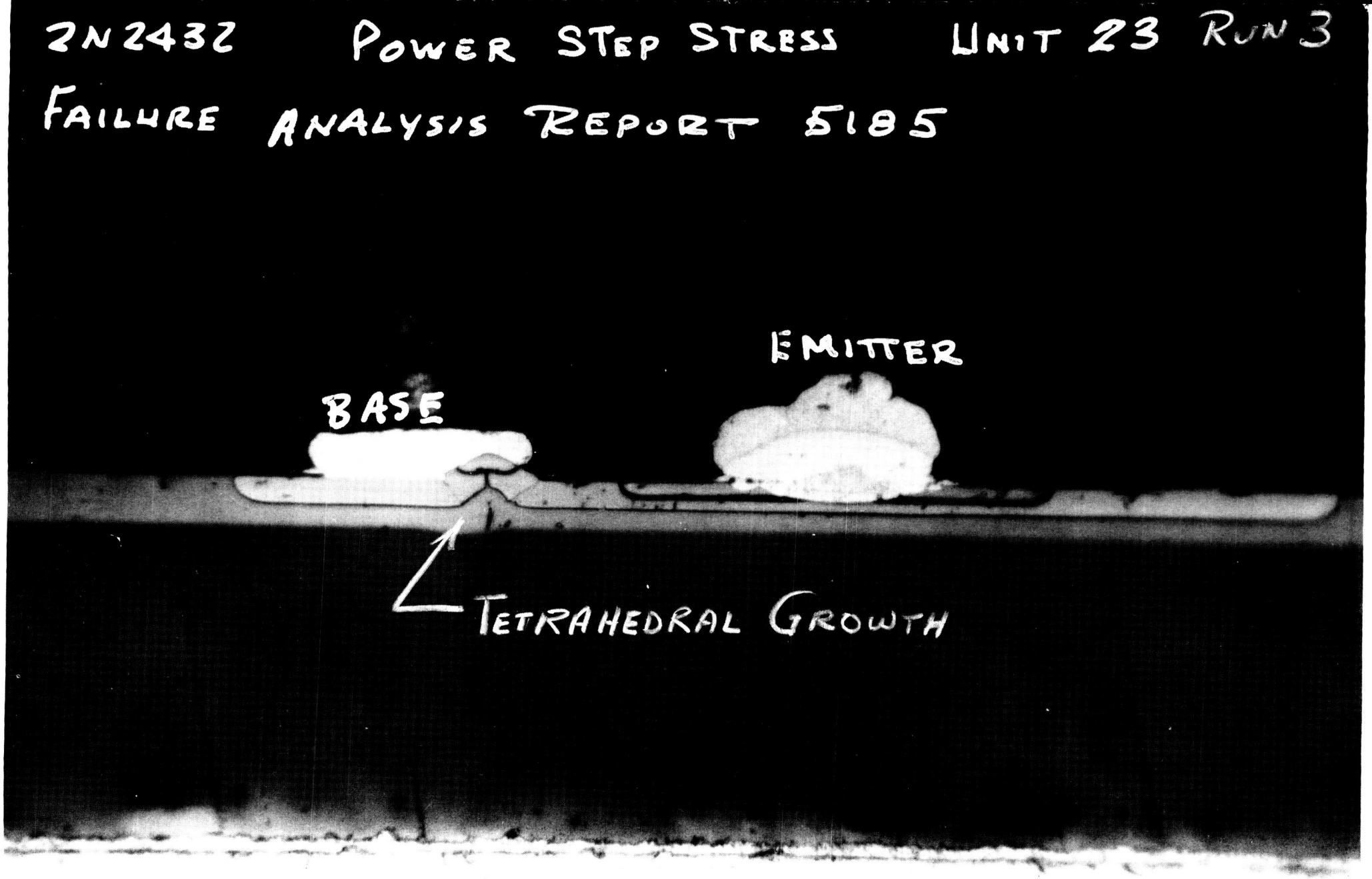


Fig. G-9 - Emitter-Base Short. Note That no Alloying Occurred at the Tetrahedral Growth

H. 1000-HOUR LIFE TEST

The original schedule called for the selection of an "optimum" materials process and a 1000-hour life test at rated power on 200 devices from this run. In view of the similarity of the step-stress test results, no optimum materials process could be identified. Consequently, it was felt that the 1000-hour life test would not yield meaningful results within the scope of the study and this phase of the proposed work was omitted.

Instead, several other tests were undertaken as described in the following sections.

I. TEMPERATURE ONLY STEP-STRESS TESTS

Since the inception of this contract one of the main considerations has been that of separating material effects from purely surface variations. A step-stress test with applied voltage (such as the one described above) is much more sensitive to surface effects than one in which stressing is done by temperature only. Because of this, and because of the few points finally available in the first test, a new test without applied voltage was initiated. Twenty units from each of the 33 runs were tested.

These units were stored for 48 hours at each of the following temperatures: 100, 125, 150, 200, 250, and 300°C. Measurements of I_{CBO}, h_{FE}, h_{fe}, BV_{CBO} and BV_{EBO} were taken on each unit at the beginning of the test and after each storage period. Test conditions are summarized in Table I-I.

These data were taken on an automatic testing machine and the IBM cards were examined to find the number of failures for each parameter. In this analysis slice, as well as deposition run, identity was maintained in order to examine differences which might exist between diffusion runs in the same batch. No significant variations in any of the parameters were observed and there were no catastrophic failures.

Table I-I - Test Conditions for Parameters Studied in the Temperature-only Step-Stress Tests

Parameter	Test Conditions
I_{CBO}	V_{CB} = 25 V, I_E = 0
h_{FE}	V_{CE} = 5 V, I_C = 1 ma
h_{fe}	V_{CE} = 5 V, I_C = 1 ma, f = 1 kc
BV_{EBO}	I_E = 10 μa, I_C = 0
BV_{EBO}	I_E = 100 μa, I_C = 0
BV_{CBO}	I_C = 10 μa, I_E = 0
BV_{CBO}	I_C = 100 μa, I_E = 0

J. 350°C STORAGE TEST

The results of the power step-stress tests lead to the tentative conclusion that there are three separate failure modes (as indicated by changes in apparent activation energy). The mechanisms of the first two are unknown but are probably surface dominated. The last was originally thought to be due to gold migration. A time versus cumulative failures test at elevated temperatures appeared to be best suited for observing this failure mode. The gold movement is very likely to be structure dependent and thus one of the few instances where material parameters might be expected to have an easily observable effect on reliability. If this is indeed the failure mode, extended storage just below the gold-silicon eutectic temperature should reveal it.

Twenty devices from each of deposition runs 2, 9, 10, 11, 12, 19, 20, 21, 22, 23, 28, 29, 31, 37 and 2-R were stored at 350°C. Measurements of h_{fe} at 1 kc, with V_{CE} = 5V and I_C = 1 ma, were made after 0, 2, 4, 8, 16, 32, 48, 70, 135, 198, and 381 hours of storage. Slice, as well as deposition run, identity was maintained so that differences between diffusion is the same fabrication batch could be detected.

There were no catastrophic failures in any of the lots tested. This suggests that the catastrophic failure mode does not depend on the formation of a Au-Si-X alloy with a melting point lower than that of Au-Si eutectic. It also suggests that local heating occurred as a result of poor thermal characteristics in the devices which failed catastrophically in the power step-stress tests.

Only four devices from the entire lot of 300 suffered as much as a 20% reduction in h_{fe}. One of these occurred after 32 hours (run 31, slice 315), two after 48 hours (run 31, slice 315 and run 2, slice 14A), and the last after 198 hours (run 2, slice 14A).

Many of the devices had improved h_{fe}. A list of those having a 20% or greater increase is given in Table J-I. Although in some cases, the value of h_{fe} reached a maximum and then fell, in no cases was there a value 20% or more lower than the initial value. These results suggest that the third non-catastrophic failure mode observed is not due to gold migration but that it, too, is probably surface dominated.

Table J-I - 350°C Storage Test

Number of devices with 20% or greater increase in h_{fe} (at 1KC)
(each lot had 10 devices)

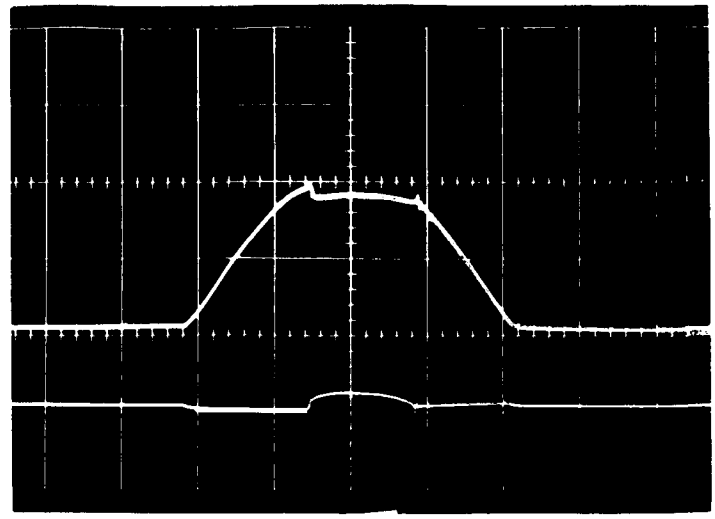
Run \ Time (hrs)	2	4	8	16	32	48	70	135	198	381
2(14A)	0	1	1	1	1	1	1	1	3	3
2(14B)	0	1	1	1	1	1	1	1	1	1
9(A3)	0	0	0	0	0	0	0	0	0	0
9(B1)	0	0	0	0	0	0	0	0	0	1
10(A1)	0	0	0	0	0	0	0	0	0	0
10(B2)	0	0	1	2	2	2	2	2	2	2
11(A1)	0	0	0	0	0	0	0	0	0	0
11(B3)	0	0	0	0	0	0	0	0	0	0
12(A3)	0	0	0	0	0	0	0	0	0	0
12(B3)	0	0	0	0	0	0	0	0	0	0
19(1)	1	1	2	3	4	4	4	4	4	4
19(3)	1	1	2	2	2	3	3	3	4	5
20(6)	0	0	0	0	0	0	0	0	0	1
20(4)	0	0	1	1	2	2	2	2	2	5
21(3)	0	0	0	0	1	1	2	3	4	5
21(2)	1	1	1	1	2	2	2	2	2	3
22(5)	0	0	0	1	1	1	1	1	3	3
22(2)	0	0	0	0	0	0	0	0	2	2
23(2)	0	0	0	0	0	0	0	0	0	0
23(2)	0	0	0	0	0	0	0	0	1	1
28(4)	0	0	0	0	3	4	6	6	7	8
28(7)	0	0	0	3	6	6	8	9	10	10
29(2)	0	0	2	4	9	9	10	10	10	10
29(3)	1	1	4	6	10	10	10	10	10	10
31(6)	0	0	0	4	9	9	9	9	10	10
31(5)	0	0	0	0	0	0	0	0	0	0
2(6)	0	0	0	0	2	4	9	10	10	10
2(3)	0	4	5	8	10	10	10	10	10	10
37(7)	0	0	1	1	1	1	2	2	2	2
37(3)	0	0	0	0	0	0	1	1	1	1

K. SECOND BREAKDOWN

A means of non-destructive measurement is provided by the second breakdown effect under conditions of limited duty cycle. A single positive half-sine wave of variable amplitude from a rectified 60-cycle line voltage was applied approximately once each second to the collector of the 2N2432 with the emitter grounded and the base open. A dual-trace Tektronix Type 545 oscilloscope was used to display simultaneously the collector-emitter voltage (SBV) waveform and the collector current (I_C) waveform. The current waveform was the differential voltage drop across a precision 100 ohm resistor in the collector circuit. Additional details of the equipment and the effect are given by Portnoy and Gamble.[12]

The amplitude of the positive half-sine wave was slowly increased until second breakdown current was observed. The amplitude was adjusted to the minimum value which would sustain second breakdown. The voltage and current waveforms under these conditions was recorded photographically on Type 47 Polaroid film. Typical waveforms are shown in Figs. K-1, K-2, and K-3. The upper curve is voltage with a scale of 10 volts per small division, the lower curve is current with a scale of 4 ma per small division, and the sweep rate is 0.4 millisecond per small division. Figures K-1 and K-2 are of the same device. A greater voltage amplitude applied in the latter case caused third breakdown. Some devices went more quickly into third breakdown as shown in Fig. K-3. In general, such devices did not display second breakdown without third breakdown.

Fig. K-1 - SBV and I_C Waveforms for a Typical 2N2432 Transistor



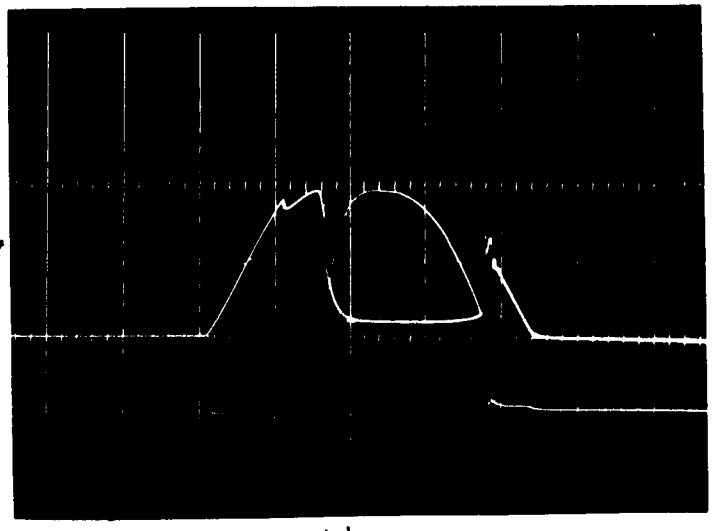
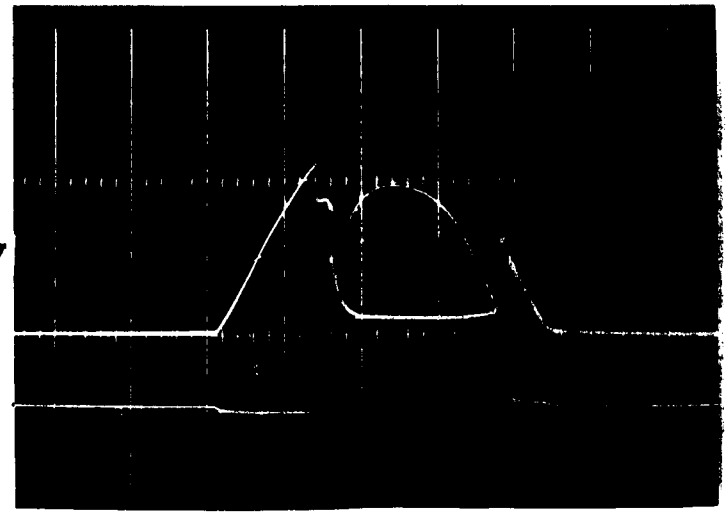


Fig. K-2 SBV and I_C Waveforms for a Typical 2N2432 Transistor Driven into Third Breakdown

Fig. K-3 - SBV and I_C Waveforms for a Typical 2N2432 Transistor Which Goes Quickly into Third Breakdown



Second breakdown voltages and currents were measured for ten 2N2432 transistors from each of two separately processed groups from runs number 2,9,10,11,12,19,20,21,22, 23,28,29,31,37, and a repeat of 2. The two groups in each run were fabricated from different slices. Usually both diffusion runs were represented. The mean values of SBV, I_C, and power with their standard deviations are tabulated in Table K-1. For convenience, graphs of SBV are shown in Fig. K-4 and of SB power in Fig. K-5.

A comparison of runs 9 and 10 with run 2, and of runs 20 and 21 with run 19 seems to indicate that SBV is reduced by either a slower or faster deposition rate than 1.5 microns per minute.

A comparison of runs 11 and 12 with run 2, and of runs 22 and 23 with run 19 suggests that a lower deposition temperature reduces SBV, but a higher temperature reduces SBV slightly.

There seems to be a small reduction of SBV with increase in dislocation density.

There is no conclusive difference in SBV between mechanical versus chemical polishing procedures.

Second breakdown voltages and currents were also measured for devices which had undergone and survived the power step-stress test series. Mean values with standard deviations of SBV, I_C, and power for slices 14A, 191, 193, and 293 of runs 2, 19, and 29 are tabulated in Table K-II.

TABLE K-I - Second Breakdown Characteristics of Unstressed 2N2432 Transistors

Run	Slice	SBV (volts)	I_C (ma)	Power (watts)
2	14A	99.8 ± 5.0	12.1 ± 1.7	1.216 ± 0.193
2	15B	94.1 ± 8.7	11.6 ± 2.2	1.096 ± 0.258
9	9A3	79.8 ± 24.0	12.9 ± 1.0	1.034 ± 0.353
9	9B1	83.2 ± 22.8	11.4 ± 2.7	0.940 ± 0.313
10	10A1	94.1 ± 26.2	14.2 ± 1.2	1.315 ± 0.342
10	10B2	82.9 ± 10.8	13.0 ± 1.8	1.074 ± 0.177
11	11A1	87.1 ± 21.0	10.3 ± 3.2	0.915 ± 0.488
11	11B3	107.0 ± 7.9	11.4 ± 1.4	1.222 ± 0.183
12	12A3	77.8 ± 5.9	10.4 ± 2.5	0.806 ± 0.040
12	12B3	63.1 ± 7.5	12.3 ± 1.7	0.767 ± 0.068
19	191	131.6 ± 4.1	12.2 ± 1.5	1.608 ± 0.232
19	193	105.4 ± 10.5	11.4 ± 0.9	1.202 ± 0.051
20	206	87.6 ± 22.7	11.1 ± 1.7	0.938 ± 0.125
20	204	64.1 ± 5.9	14.2 ± 1.0	0.907 ± 0.074
21	213	102.5 ± 5.6	11.4 ± 1.4	1.166 ± 0.138
21	212	80.1 ± 11.4	12.8 ± 1.2	1.026 ± 0.185
22	225	111.0 ± 9.4	9.5 ± 0.8	1.053 ± 0.109
22	222	94.6 ± 2.6	9.8 ± 0.9	0.928 ± 0.094
23	232	70.3 ± 24.2	15.8 ± 5.3	1.001 ± 0.151
23	232	60.6 ± 20.7	18.8 ± 4.4	1.005 ± 0.091
28	284	112.2 ± 8.2	8.7 ± 0.8	0.970 ± 0.045
28	287	125.6 ± 4.9	7.4 ± 0.5	0.930 ± 0.085
29	292	86.9 ± 4.8	11.1 ± 0.9	0.963 ± 0.082
29	293	83.1 ± 4.0	10.7 ± 0.9	0.890 ± 0.095
31	316	93.2 ± 4.0	8.7 ± 1.1	0.813 ± 0.120
31	315	104.4 ± 12.9	10.4 ± 2.8	1.118 ± 0.441
37	377	116.0 ± 12.8	9.6 ± 0.7	1.113 ± 0.144
37	373	86.3 ± 5.7	10.5 ± 1.4	0.903 ± 0.110
2	26	103.1 ± 2.9	10.5 ± 1.1	1.083 ± 0.123
2	23	98.6 ± 4.2	10.4 ± 0.5	1.024 ± 0.047

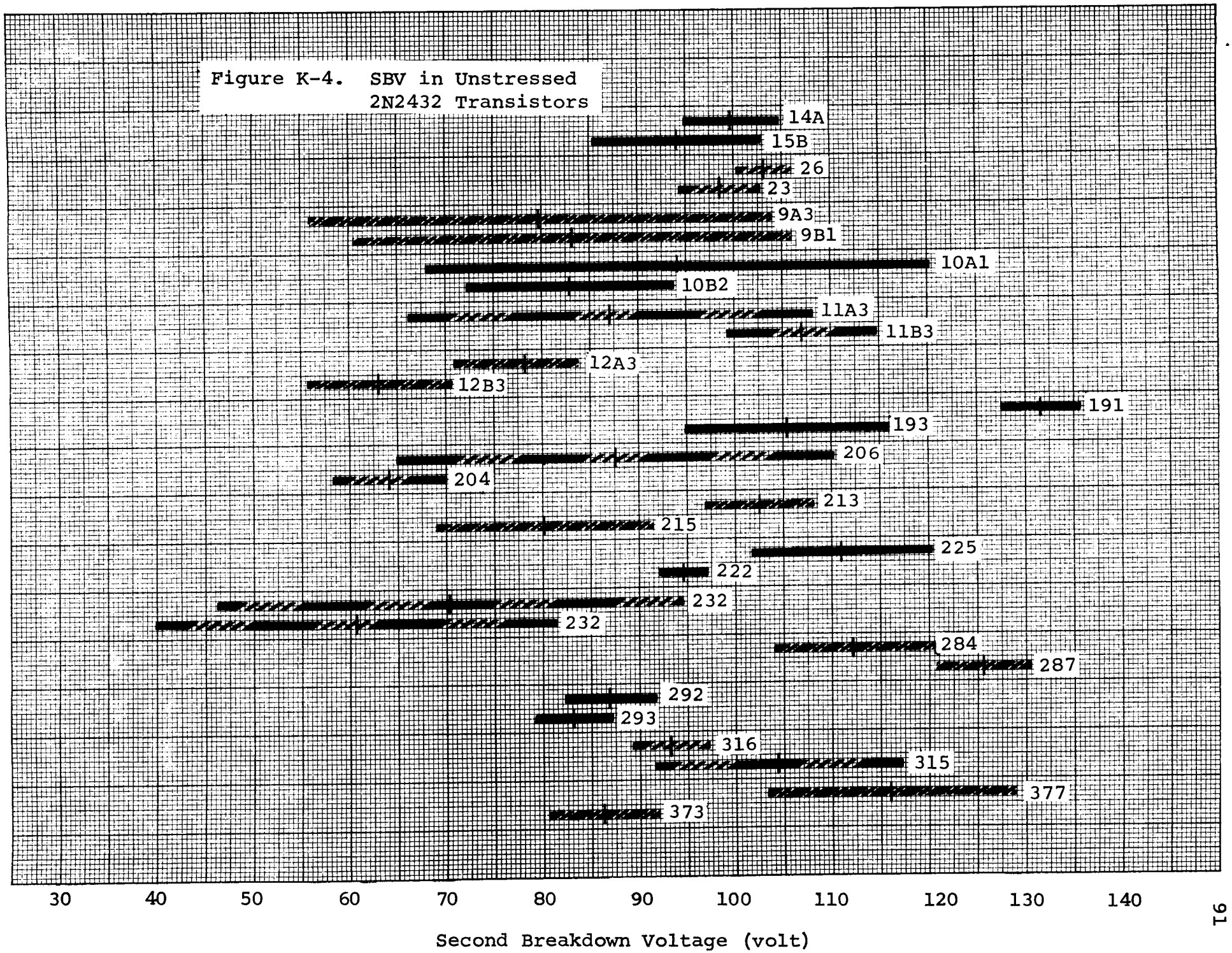


Figure K-4. SBV in Unstressed 2N2432 Transistors

Figure K-5. SB Power in Unstressed 2N2432 Transistors

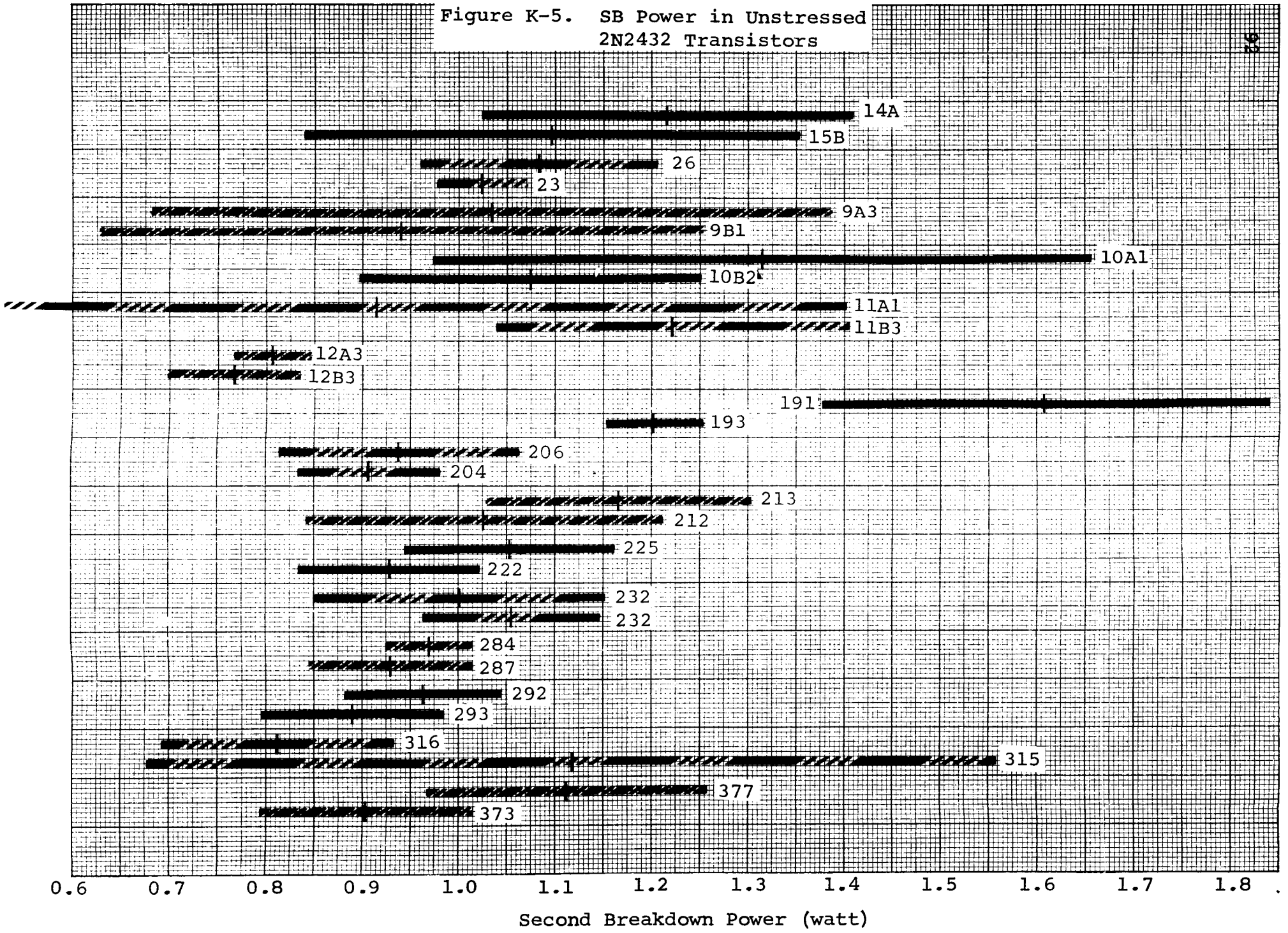


TABLE K-II - Second Breakdown Characteristics of Power Step-Stressed Transistors

Run	Slice	SBV (volts)	I_C(ma)	Power (watts)
2	14A	92.0 ± 8.4	10.0 ± 1.1	0.916 ± 0.088
19	191	57.0 ± 19	18.0 ± 5.5	0.929 ± 0.108
19	193	91.1 ± 10.7	11.1 ± 3.6	0.994 ± 0.130
29	293	82.8 ± 6.6	11.0 ± 2.0	0.897 ± 0.079

TABLE K-III - Second Breakdown Characteristics of High-Temperature-Storage Stressed Transistors

Run	Slice	SBV (volts)	I_C(ma)	Power (watts)
2	14A	91.9 ± 9.6	11.2 ± 1.4	1.024 ± 0.130
19	191	100.6 ± 24.6	11.2 ± 2.3	1.125 ± -.154
19	193	97.8 ± 3.5	9.7 ± 2.5	0.947 ± 0.058
29	293	75.6 ± 1.3	11.6 ± 0.7	0.877 ± 0.053

The devices which had undergone the power step-stress tests had a slightly reduced SBV and SB power. Those from slice 191 had a very low SBV with an increased I_C The reason for this is not clear, but it was not unexpected since the values for BV_{CEO} in the devices from this slice which were power stressed were much lower than the values in the unstressed samples. There were only five surviving devices in the power stressed sample from slice 191 (as contrasted with the very high survival rate of that from slice 193). It should be noted that the power stressed devices from runs 2 and 19 were subjected to an extra stress period of 72 hours at 800mw.

A third group of SB measurements was made for devices which had undergone the high temperature storage test. Mean values with standard deviation of SBV, I_C, and power for groups 14A, 191, 193 and 293 from runs 2, 19, and 29 are tabulated in Table K-III.

A comparison of SBV for the unstressed, power step-stressed and high temperature storage stressed transistors from slices 14A, 191, 193, and 293 is shown in Fig. K-6. Figure K-7 compares SB power for the same devices.

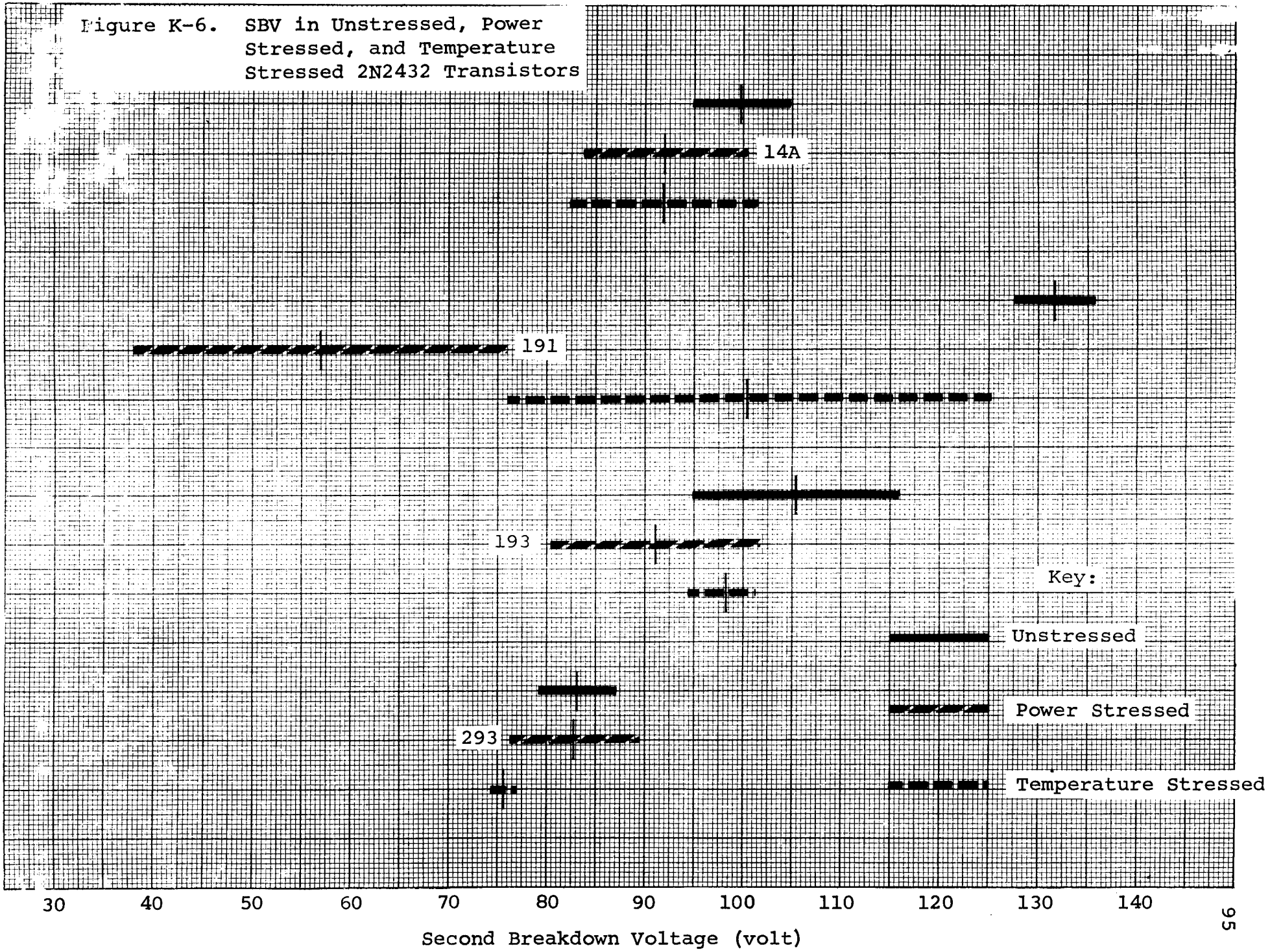
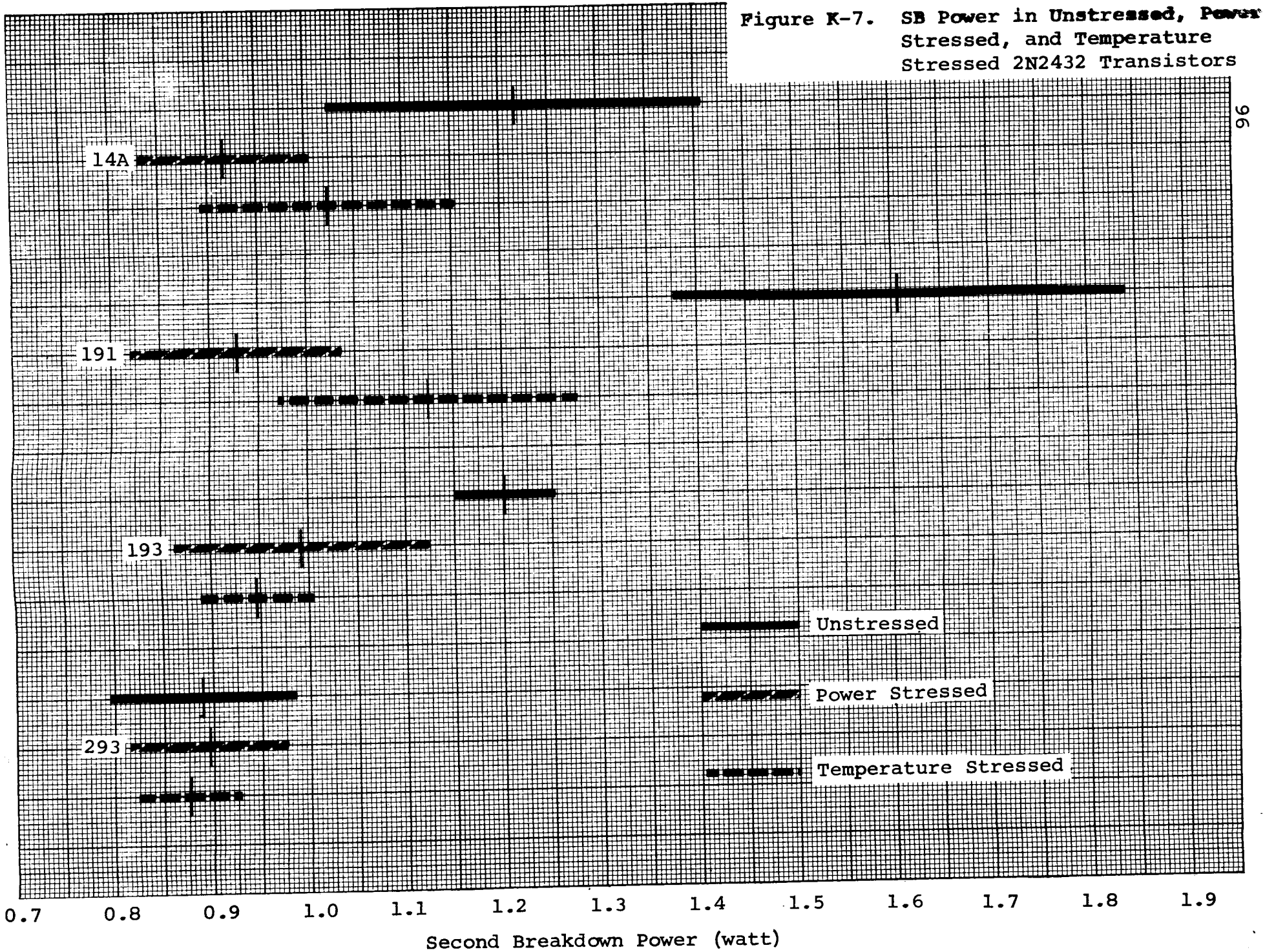


Figure K-6. SBV in Unstressed, Power Stressed, and Temperature Stressed 2N2432 Transistors

Figure K-7. SB Power in Unstressed, Power Stressed, and Temperature Stressed 2N2432 Transistors



L. MODELS FOR DEVICE CHARACTERIZATION

In order to examine bulk-surface-device parameters relationships it is necessary first to have some mathematical models which include both bulk and surface measurable quantities and the various device parameters of interest. Unfortunately, few such models exist, and they are by and large rather unreliable themselves. Moreover, it can be seen as they are developed that most of the models are so involved, and so few of the parameters actually known, that interpretation is difficult. Interpretation is also hampered because many of the equipments used to measure transistor parameters do not uniquely respond to a particular one, and unless care is taken, changes in readings may be attributed to the wrong parameter. This pitfall can be minimized by individually checking each device, but if large quantities of devices are to be studied, the time is prohibitive.

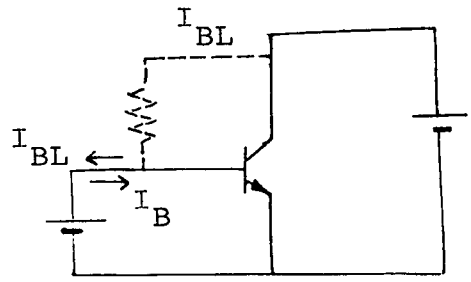
For example, if I_{CBO} increases appreciably because of surface effects it may bring about an apparent increase in h_{FE} (grounded emitter dc current gain). Consider the diagram in Fig. L-1. With no leakage

$$h_{FE} = \frac{I_C}{I_B} ,$$

where I_C and I_B are the ideal collector and base currents respectively. If there is a leakage current, $I_{BL} = I_{CBO}$, the collector current is increased while the measured base current is decreased:

$$h'_{FE} = \frac{I_C + I_{CBO}}{I_B - I_{CBO}} .$$

Fig. L-1 - Effect of I_{CBO} Changes on h_{FE}.



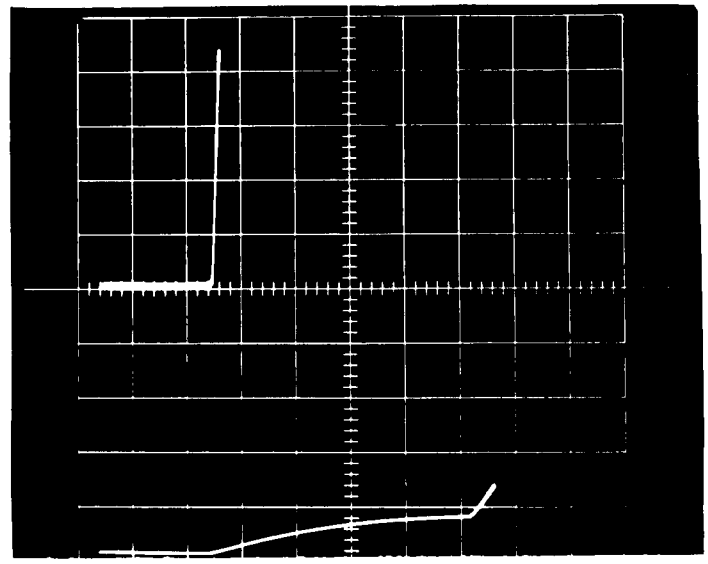


Fig. L-2 - Reverse Current Voltage Oscillogram of a Transistor Collector-Base Junction. Both curves have the same horizontal scale of 5 volts/div. The vertical scale for the lower curve is 2 ma/div., while that for the upper is 0.1 ma/div.

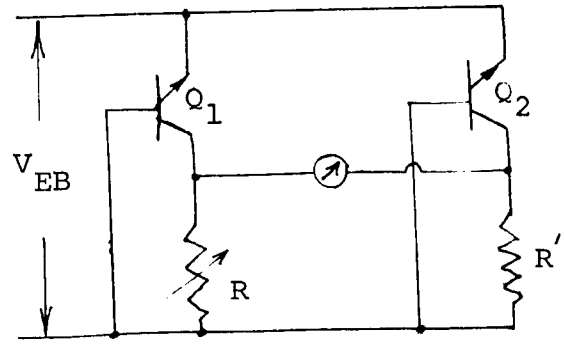


Fig. L-3 - Temperature Compensating Bridge Circuit for Measurement of Collector Current.

Note that if the transistor were operated grounded base, and α determined by a direct measurement of I_E and I_C, the effect would be much less noticeable. The power step-stress data included a measurement of h_{FE}, and the correlation between it and I_{CBO} which was observed was probably due to this effect. AC measurements eliminate this difficulty and were substituted in subsequent tests.

Another instance of interpretation difficulty arises in the machine measurement of BV_{CBO}. Surface effects usually greatly increase I_{CBO}, and the result can be interpreted as a reduced breakdown when in fact it is not. For example, the two I-V curves of Fig. L-2 illustrate this. The curve on the bottom was taken with a rather reduced current sensitivity and shows severe rounding near the breakdown knee, and an apparent BV_{CBO} of 37 volts. The top curve in the photograph (of the same device) has had the current gain increased and appears to show a sharp break but at a much lower voltage. If BV_{CBO} were measured and recorded (and it usually is) as the voltage at a specified current, then the measured value will be sensitive to I_{CBO}. Some measurements of this effect can be obtained by recording a "breakdown voltage" not at just one current, but at several. Thus, if a softening occurs it can be detected. This also was done in the second step-stress test series.

1. Current Gain (α)

The simple small signal expression for α is usually given as

$$\alpha = \beta\gamma\alpha^*$$

where β is the transport efficiency,
γ is the emitter efficiency, and α^*
the collector multiplication factor.

$$\beta \approx 1 - \frac{w_o^2}{2L_n^2}$$

$$\gamma = 1 - \frac{D_p N_A L_n}{D_n N_D L_{pE} \coth \frac{w_o}{L_n}} \approx 1 - \frac{D_p N_A w_o}{D_n N_D L_{pE}}$$

$$\alpha^* \approx 1$$

where w_o = width of base between the inside edges of base collector and base-emitter transition region

D_n, L_n = diffusion coefficient and diffusion length of minority carriers in base

D_p, L_{pE} = diffusion coefficient and diffusion length of minority carriers in emitter

N_D = impurity concentration in emitter

N_A = impurity concentration in base

While this expression is useful in considering the effect of bulk parameter changes on α, it does not include surface terms. Such effects can arise in many ways; for example, surface leakage across the collector-base junction can give an apparent enhancement of h_{FE} (but not α). Surface effects which change the diode behavior can degrade low current γ, surface recombination currents will cause a decrease of β, as will volume recombination.

By following Webster's analysis[27] of h_{FE} variation with emitter current, a surface recombination term affecting β can be introduced. This can be done in a rudimentary fashion and gives

$$\alpha \approx 1 - \frac{w_o^2}{2D_n \tau_n} - \frac{A_S^n w_o S^n}{A D_b} - \frac{1}{1 + \frac{N_{DE} L_{pE} D_n}{N_A w_o D_p}} \qquad (1)$$

where S is the surface recombination velocity,

A_S is the area of recombination,

A is the cross section of the device, and

superscript n represents the normal transistor connection.

The expression for inverse α is very similar, but the area active in surface recombination may now be different, and of course since the collector-base junction is now emitting, $N_{DE} \rightarrow N_{DC}$ and $L_{pE} \rightarrow L_{pC}$. These changes give:

$$\alpha_I \approx 1 - \frac{w_o^2}{2D_n \tau_n} - \frac{A_S^i w_o S^i}{A D_n} - \frac{1}{1 + \frac{N_{DC} L_{pC} D_n}{N_A w_o D_p}}$$

where superscript i represents the inverse transistor connection.

There is still another correction that is sometimes necessary.[28] It is caused by recombination current in the emitter junction. Any such currents do not contribute to minority carriers within the base and hence decrease the emitter efficiency. That is

$$\alpha = \frac{J_{nE}}{J_{nE} + J_{pE} J_r} = \frac{1}{1 + \frac{J_{pE}}{J_{nE}} + \frac{J_r}{J_{nE}}}$$

where J_{nE} is the electron current

J_{pE} is the hole current

J_r is the recombination current,

This equation may be put into a more standard form and becomes

$$\alpha = 1 - \frac{D_p N_A w_o}{D_n N_{DE} L_{pE}} - \frac{J_r w_o N_A}{n_i^2 q D_p} e^{-\frac{qV_{EB}}{kT}} \qquad (2)$$

If the effects introduced in arriving at Eq. (2) are added to the already complicated expression for α given in Eq. (1):

$$\alpha \approx 1 - \frac{w_o^2}{2D_n \tau_n} - \frac{A_S^n w_o S}{A D_n} - \frac{N_A w_o D_p}{N_{DE} L_{pE} D_n} - \frac{J_r w_o N_A e^{-\frac{q V_{EB}}{kT}}}{n_i^2 q D_p} \qquad (3)$$

It should be noted that in Eq. (3), the assumption is made that each of the terms is very small. For most cases of forward operation this is true. In the inverse configuration however, α may become the order of 0.3 to 0.5. Equation (1) accounts for this in a simplified way, but does not add the recombination term.

2. Collector Current (I_C)

Rather than attempt to separate the bulk from surface terms by analyzing the device behavior under varying conditions, it seems possible, by following a procedure suggested by Benda,[13] to afford a separation by the mode of measurement. Recall that simple theory (neglecting surface effects) specifies that the emitter and collector currents can be written as

$$I_E = a_{11}\left[\exp\left(\frac{q V_{EB}}{kT}\right) - 1\right] + a_{12}\left[\exp\left(\frac{q V_{BC}}{kT}\right) - 1\right]$$

$$I_C = a_{21}\left[\exp\left(\frac{q V_{EB}}{kT}\right) - 1\right] + a_{22}\left[\exp\left(\frac{q V_{BC}}{kT}\right) - 1\right]$$

$$a_{21} = -kT \frac{A\mu_n}{L_n} \frac{n_i^2}{N_A} \frac{1}{\sinh \frac{w_o}{L_n}}$$

$$a_{11} = kTA\left[\frac{\mu_n n_i^2}{L_n N_A} + \frac{\mu_p n_i^2}{N_{DE} L_{pE}}\right]$$

$$\gamma\beta = \frac{a_{21}}{a_{11}} \approx \alpha.$$

If V_{BC} is reduced to zero, then $I_C = a_{21} \left[\exp\left(\frac{q\, V_{EB}}{kT}\right) - 1\right]$. But keeping V_{BC} zero also eliminates any surface leakage from base to collector. Contributions due to recombination current will also be eliminated, so that the measured I_C is indeed a function only of a_{21}. If I_C is now monitored at a fixed V_{EB} throughout a step-stress test, and remains constant, then any changes in α are due to surface changes.

There are however, a few inherent difficulties with such a test. First, if the contact resistance changes, then (V_{EB} actual) will change, and can thus affect I_C. If I_C is read at only one voltage there is no way to detect or separate changes of resistance from changes in a_{21}. When I_C read as a function of V_{EB} is plotted logarithmically, regions which yield a straight line are assumed to be independent of spurious effects. It is, however, tedious to plot such a curve for many devices, and in the actual data taken this was not done. This was unfortunate because one of the devices tested showed an abrupt decrease in calculated a_{21} which could not be associated with similar changes in α, and was ascribed to the series resistance effect. The second difficulty arises because of the high accuracy required in the measurement of V_{EB} and I_C in order to observe small changes in h_{FE}* when it is above 100. The problem is particularly difficult because of the large temperature coefficient of I_C versus V_{EB}.

In some measure, the problems were reduced by using the bridge of Fig. L-3. Transistor Q_2 was used as a standard and not subjected to the step-stress testing. The resistors R and R' were a fraction of an ohm so that V_{BC} was never more than

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* $h_{FE} = \alpha/(1-\alpha)$

1 millivolt. At balance:

$$I_C^1 = A \frac{R'}{R} I_C^2$$

but also,

$$\frac{I_C^1}{I_C^2} = \frac{a_{21}^1}{a_{21}^2} .$$

Thus, if a_{21}^1 and a_{21}^2 have the same temperature functional form the bridge will remain balanced as temperature varies. Similarly, if V_{EB} changes, the bridge should remain balanced, except for series resistance in the emitter-base circuit. If it is assumed that a_{21}^2 remains constant, then

$$a_{21}^1 = a_{21}^2 A \frac{R'}{R}$$

and

$$\frac{\bar{a}_{21}^{-1}}{a_{21}^1} = \frac{R}{\bar{R}}$$

where the bars represent subsequent readings of the same device.

Even with this arrangement there were small deviations which could only be ascribed to temperature imbalance. The normalized results are shown in Table L-I.

3. Reverse Current (I_{CBO})

I_{CBO} is written in simplified form as

$$I_{CBO} = q\, n_i^2\, A \left[\frac{D_p}{L_p N_D} + \frac{D_n}{w_o N_A} \right], \tag{4}$$

If surface leakage paths are taken into account, and written inclusively as I_{SL}, and if recombination within the space charge region is added

$$I_{CBO} = \frac{n_i v}{\tau} + I_{SL} + q\, n_i^2 \left[\frac{D_p}{L_p N_D} + \frac{D_n}{w_o N_A} \right],$$

where v is the volume in which recombination occurs, and I_{SL} is the surface term. The volume v will vary with voltage in a manner determined by the impurity gradient, but will be approximately as $V_C^{1/2}$.

Table L-I - Normalized Values of Resistance R in the Circuit of Fig. L-3 for 10 Units Stored at 350°C for the Time Shown

Time hrs / Unit	0	2	4	8	16	32	48	70	135	198	381
104	1	.987	.996	.996	1.004	.986	.986	.985	.986	.987	.980
108	1	.987	.980	.983	.985	.972	.980	.983	.983	.985	.992
112	1	.977	.985	.984	.991	.987	.980	.988	.979	.979	.980
116	1	.979	.982	.989	.988	.971	.977	.967	.965	.973	.988
120	1	.978	.982	.979	.982	.981	.990	.979	.977	.986	.982
224	1	.999	.989	.993	.994	.994	.994	.992	.996	1.005	1.005
228	1	.984	.988	.990	.993	.979	.997	.990	.988	.996	.994
232	1	.984	.992	.868	.872	.861	.872	.880	.892	.906	.914
236	1	.988	.985	.985	.988	.969	.981	.981	.976	.984	.976
240	1	.984	.990	.991	.998	.981	.979	.986	.986	.991	1.000

4. Collector-base Breakdown Voltage (BV_{CBO})

Usually the collector-base breakdown voltage is considered to be a function only of the resistivity ($\approx \rho^n$), but surface leakage and microplasmas are known to reduce the measured breakdown. However, if the microplasmas are of small area and carry little current, they will appear only to cause an increase in I_{CBO}. As a very rough expression for BV_{CBO} one might write the following three equations in order to account sequentially for avalanche in the bulk, increased leakage affecting the measured voltage, and microplasmas:

$$BV_{CBO} = C_1\rho^n \quad \text{("perfect" material)}$$

where C_1 is a constant and n usually is between .5 and 1.5

$$BV_{CBO} = C_1\rho^n - C_2I_{CBO}$$

$$BV_{CBO} = C_1\rho^n - C_2I_{CBO} - C_3\Sigma a_i$$

where I_{CBO} is assumed to be primarily the surface leakage and a_i is the area of the ith microplasma. However, the microplasma can only reduce the over-all voltage to that determined by its own breakdown voltage. This voltage may only be slightly below the bulk value, or as small as a few volts, depending on what flaw

produced the microplasma. To take this into account.

$$BV_{CBO} = C_1\rho^n - C_2 I_{CBO} - C_3\Sigma a_i\Delta v_i$$

where Δv is the difference between bulk breakdown voltage and that in the microplasma area. Admittedly such linear combination are very naive, but qualitatively predict the direction of the change to be expected.

5. Emitter-collector Shorts

The direct cause of shorts is generally the emitter contact metal developing spikes which reach down to the collector. It is also sometimes observed that the spikes originate at the collector-header bond and go all the way through the thick collector region and into the base (and/or emitter).

The cause of the metal migration has not been determined, so some theorizing is in order. Localized heating up to the metal-silicon eutectic temperature can cause such spikes, and if the device is subjected to a sudden overload, such a mechanism is understandable. However, growth of a spike under such circumstances should be quite rapid. In order to explain the slower process (up to several days at excessive rating) often observed, a more subtle process is indicated. Surface migration into surface cracks might occur for example, and it would then proceed slowly as cracks grow. Diffusion

coefficients may be enhanced in damaged regions (dislocations, along slip boundaries, stacking faults). It should be noted however that a cross section through a device which failed by a spike from the emitter did not have the spike at a "tetrahedron" defect which was covered by base metalization. The tetrahedron involves twin lines, stacking faults, and stair rod dislocations, and represents a fairly severe collection of defects. On this meager data one concludes that the standard crystallographic defects are not necessarily the most important ones, and that one should look further. It may be that the localized hot spot mentioned earlier does materialize as contacts deteriorate. There is also the possibility that local impurities mix with the contact material to form a ternary (or higher) compound with a liquidus temperature far below that predicted from the binary system. Since source material would be limited, such a process might be expected to progress slowly. In an effort to formulate an expression for the incidence of shorting it seems reasonable to include the thermal resistance from the wafer to header; the number of serious lattice defects (even they may be only of secondary importance); the power dissipation; thermal gradients and resistivity gradients. This suggests that:

$$P(s) = \frac{r\ A\ W\ C_1}{w_E} \left|\frac{d\theta}{dR}\right| \left[C_2 B + C_3 F + C_4 N + C_5 \left|\frac{dp}{dR}\right|\right],$$

where $P(s)$ = probability of a short

r = thermal resistance of assembly

A = cross sectional area of the device

W = power being dissipated

C_i = constant

w_E = distance from metal contact to E-B junction

$\frac{d\theta}{dR}$ = maximum local temperature gradient

$\frac{dp}{dR}$ = maximum local resistivity gradient

6. Emitter Current (I_E)

The current-voltage relationship for a forward biased emitter junction is usually given as

$$I_E = I_O \left[\exp\left(\frac{qV}{kT}\right) - 1 \right]$$

where I_O is identical with I_{CBO} of Eq. (4). This expression is based in diffusion current only and does not include high level injection or space charge region recombination current. The recombination current will add a term proportional to $\exp \frac{qV}{nkT}$ so that

$$I_E = I_O \exp\left(\frac{qV}{kT}\right) + I' \exp\left(\frac{qV}{nkT}\right)$$

where n is usually between 1 and 2, but often is as much as four. This term can change with time if the junction area changes because of the growing or diminishing of inversion layers. The centers that cause the recombination current are not necessarily uniformly distributed across the emitter cross section, and indeed it has been suggested that much of this excess current originates near the periphery of the emitter in planar transistors. If this is true, any change which perturbed the current distribution in the device would cause a change in the recombination current.

7. Individual Parameters Contributing to Models

From those models just listed, a tabulation of the individual properties can now be made and is given in Table L-II. With this list, the problem now becomes one of determining which of the many properties might change and how such changes affect transistor behavior. The complexity of the models, their incompleteness, and the number of variables just tabulated (and about whose behavior little is known) leads to the conclusion that except for the method of observing changes in a_{12} described in section L-2, it is not presently feasible to interpret parameter changes in terms of the individual contributors.

Table L-II - List of Individual Parameters Contributing to Models

Collector Region	Base Region	Emitter Region
$N_{DC}(x)$	w_o	$N_D(x)$
L_pC	$N_A(x)$	L_{pE}
μ_{pC}	$\int N_A(x)\,dx$	μ_{pE}
μ_{nC}	L_n	μ_{nE}
w_C-collector width		w_E

N = density of precipitates

F = stacking fault density

B = dislocation density

T_T = material stress due thermal

T_M = material stress due to mechanical constraints

S = surface recombination

A_S = area with surface recombination

T_{IE} = stress due to heavy impurity concentration in emitter

$\theta(y,z)$ = temperature distribution

$R(\theta, N_p, F_C, T_I, T_M, N_B, B)$ = rate of solution of silicon by contact

$I(x)$ = density of deep level impurities

p = number of dipoles/unit area on the surface

Γ = ratio of width of space change region at surface to width in body of device

W_{d-b} = collector-base depletion width

W_{e-b} = emitter-base depletion width

M. NEW TECHNOLOGY

The study reported here did not require the development of new technology for its pursuit. No new technology was developed during the course of the work.

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under power stressing result dominantly from surface effects. No pattern which could be assigned to epitaxial deposition parameters was observed.

4. Present epitaxial deposition techniques appear to be a relatively non-critical factor in the fabrication of low-voltage, small signal devices of the type examined in this study. Any correlation which may exist between epitaxial deposition parameters and device reliability could not be demonstrated by these studies. It cannot be assumed that studies on other types of devices (e.g., narrower base, higher voltage, higher power) would not exhibit such correlation.

5. The usefulness of the non-destructive techniques of x-ray topography and second breakdown measurements in future work of this type was indicated during the later stages of this study.

6. From the preliminary topographic studies reported, it can be concluded tentatively that the grinding operation associated with the (110) flat on a typical silicon crystal introduces strain which manifests itself in large densities of dislocations after heat treatment such as the crystal receives during epitaxial deposition.

7. The preliminary non-destructive second breakdown studies showed minor differences between devices as initially fabricated and similar devices after being power stressed. Such differences were also observed in the case of devices which have been subjected to higher temperatures only.

8. The influence of an in-reactor vapor etch in reducing the stacking fault density in epitaxially deposited films was confirmed.

9. During the course of this study it became apparent that highly specialized device structures and circuitry would be required to separate surface and bulk effects. Some very crude beginnings along these lines were made but much remains to be done in this area. It can also be concluded that simultaneous examination of such a wide range of variables will not lead to conclusive results in studies of this type.

B. RECOMMENDATIONS FOR FURTHER STUDY

1. Additional work to determine the conditions under which the defect density in an epitaxial film influences device reliability should be undertaken. Special device structures and measurement techniques designed to eliminate the influence of surface and fabrication variations should be employed.

2. Further study of the gold-alloying mechanism should be undertaken to establish if it is enhanced by the presence of defects in the epitaxial layer or by the existance of electric fields encountered during device operation.

3. Further second breakdown studies on specialized device structures stressed in various ways are likely to prove useful in establishing correlations between deposition conditions and device characteristics and reliability.

4. Use of device structures specially designed to eliminate failures due to surface conditions is recommended for future studies of this type. High-voltage, high-power devices appear to be more likely to exhibit correlations than small-signal devices and it is suggested that future studies be oriented toward devices of this type.

5. The effect of material parameters on surface instability should be explored. For example, the crystallographic orientation of the substrate may affect the properties of the oxide grown on it, or impurities originally in the silicon may segregate at the surface during the processing and adversely affect device performance.

6. The possibility that thermally induced stresses or excessive contact pressures may lead to phase changes of the semiconductor itself, or to changes in the character of the various contact-semiconductor phase diagrams should be investigated.

7. It is recommended that fewer variables be included in future studies of this type in order that the effects of the most significant variables may be more fully examined and understood.